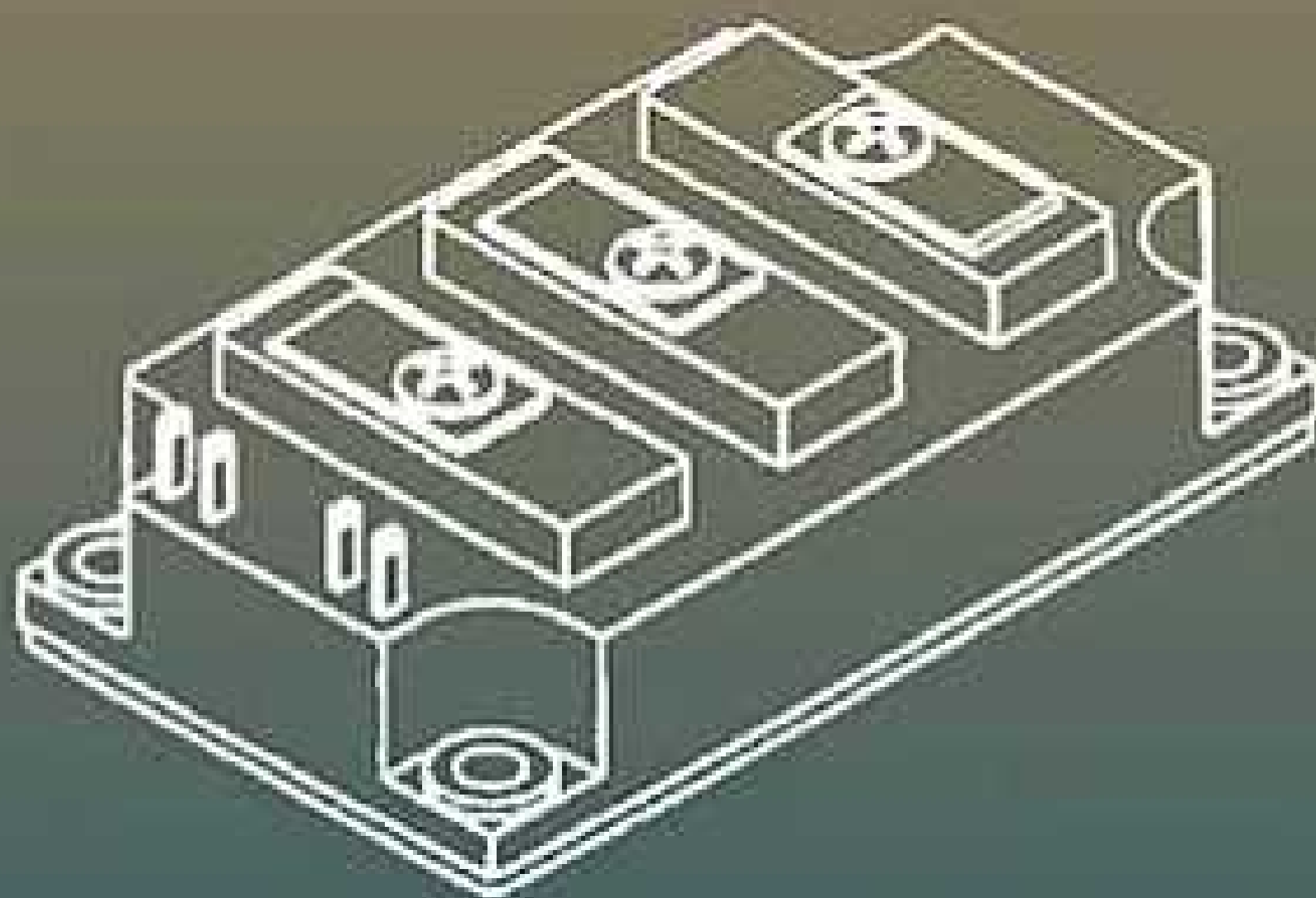


POWER ELECTRONIC MODULES

DESIGN AND MANUFACTURE



WILLIAM W. SHENG
RONALD P. COLINO



CRC PRESS

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Boca Raton London New York Washington, D.C.

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Library of Congress Cataloging-in-Publication Data

Sheng, William W.

Power electronic modules : design and manufacture / William W. Sheng, Ronald P. Colino.
p. cm.

Includes bibliographical references and index.

ISBN 0-8493-2260-X (alk. paper)

1. Power semiconductors—Design and construction. I. Colino, Ronald P. II. Title.

TK7871.85.S522 2004

621.381—dc22

2004053697

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International Standard Book Number 0-8493-2260-X

Library of Congress Card Number 2004053697

Printed in the United States of America 1 2 3 4 5 6 7 8 9 0

Printed on acid-free paper

Preface

A power semiconductor module is basically a power circuit of different materials assembled together using hybrid technology, such as semiconductor chip attachment, wire bonding, encapsulation, etc. The materials involved cover a wide range from insulators, conductors, and semiconductors to organics and inorganics. Since these materials all behave differently under various environmental, electrical, and thermal stresses, proper selection of these materials and the assembly processes are critical. In-depth knowledge of the material properties and the processing techniques is therefore required to build a high-performance and highly reliable power module.

Designing and building power semiconductor modules requires an integration of different technologies. Engineers need to possess basic knowledge of the following:

- Semiconductor chip
- Thermal-electrical and thermal-mechanical management
- Ceramic substrate and metallization
- Metallic baseplate
- Solder and soldering techniques
- Solder bump technology
- Plastic materials
- Power terminals
- Cleaning chemistry and technology
- Ultrasonic aluminum wire bonding
- Epoxy and coating
- Environmental constraints
- Electrical, thermal, and mechanical testing
- Inspection techniques and tools
- Analytical techniques and tools
- Reliability, statistical process control, highly accelerated life testing (HALT), highly accelerated stress screen (HASS), and life tests
- Facilities requirements
- Barcode or 2D data matrix symbol

This diversity represents a challenge. This book is an attempt to address these needs of the rapidly growing body of engineers involved in the power semiconductor module product. It is impossible to cover the details of each of these technologies in a single book. Here, based on their past experience,

the authors have presented the essential segments of each technology. This represents the basic knowledge or fundamentals required.

Power IGBT (insulated gate bipolar transistor) module is gaining a great deal of interest lately because of its growing importance in the power industry, especially in the fields of power generation, power conversion, UPS (uninterrupted power supply), welding, robot, automotive, and AC/DC motor drive. Due to its rising popularity, power IGBT modules will be the focus of discussion throughout this book, although the general technology is applicable to other types of power modules as well. Most power semiconductor OEMs (original equipment manufacturers) are currently either already producing or in the process of actively developing this IGBT product. A great deal of research in this field has also been conducted in universities. As a result, numerous articles have been published in technical journals and also presented in many power conferences. This represents a vast amount of useful but scattered information. Therefore, in addition to establishing the basic foundation for power module design and manufacturing, the authors have built upon the latest developments and presented those that are considered appropriate.

Although this book specifically addresses thermal management of power IGBT modules, the knowledge presented is generally applicable to thermal management of most electronic products. As function and power density are increasing in almost all facets of the electronics industry, thermal management has become ever more important to ensure long-term reliability. This includes thermal management of electronic products from consumer electronics through military/aerospace applications. Areas of application may include RF transmitters, cell phones, microprocessors, memories, automotive products, portable/hand held electronics devices, etc. The information presented here is applicable to these and many more electronics projects.

The book is organized into three basic sections:

- Materials
- Manufacturing processes and quality control
- Design and results

In each section, the emphasis is on the practical aspect. The intention is to allow the readers to apply this information directly to their work or study.

Throughout the book, names of companies that supply certain materials and equipment or that provide specific services are listed. These names are meant only as reference and do not represent any endorsement by the authors.

This book is intended to serve:

- Design, process, quality control, and application engineers working with power modules
- Researchers and university students in the field of power electronics

Authors

William W. Sheng is a cofounder of Smart Relay Technology, Inc., where he has served as vice president of engineering. He has been in the electronics industry for over 25 years, specializing in solid-state relay and power semiconductor technologies. After his graduate study, he was on the engineering staff of General Electric Power Semiconductor Department where he was involved in the design and manufacturing of power semiconductor chips and modules. Prior to Smart Relay Technology, he was the manager of a power hybrid division where he led the development of the PhotoMOS solid-state relay. He has received the Inventor Award from General Electric. He is the author of numerous articles and holds several patents in the semiconductor field.

Ronald P. Colino is a cofounder of Smart Relay Technology, Inc., serving as president for the past 13 Years. A graduate of Manhattan College School of Engineering, Colino has worked in the electronics industry for over 40 years. Part of this time has been as memory products manager at General Instruments Microelectronic Division. His experiences include design and marketing of solid-state relays, hybrid integrated circuits, MOS integrated circuits, and semiconductor memories. Colino is a member of IEEE and the author of several technical papers. He holds several patents in the integrated circuit field.

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Dedication

*Dedicated to Lord Jesus without whose presence this book would not be possible
and to Helen for her constant support.*

William Sheng

To Wilma, with love.

Ronald Colino

1

Introduction

A basic power semiconductor module consists of a stack of four main (or first-order) parts (see [Figure 1.1](#)):¹

- Power semiconductor chips
- Insulating substrate with metallization (circuit conductor)
- Baseplate
- Bonding material

Each of these parts is of a different material:

- **Power semiconductor chips** — Si (IGBT, FRED, MOSFET, Thyristor, Rectifier)
- **Insulating substrate** — Usually ceramic or Si-based substrate with Au, Ag, or Cu with metallization (metallizations deposited on top or both surfaces)
- **Baseplate** — Cu metal, Cu composites, carbon-reinforced composites, AlSiC, etc.
- **Bonding material** — Typically Pb-based soft solder, Pb-free solder, etc.

In addition, there are also three second-order materials involved:

- **Encapsulant** — Typically conformal coating for environmental and mechanical protection
- **Power interconnections** — Large Al wire for interconnections, pressure-type contact, and metal terminals
- **Plastic case and cover** — Thermoset and thermoplastic material

These materials are in intimate contact with each other because they are all bonded together. Since the materials behave differently under various environmental electrical and thermal stresses, proper selection is vital to the success of the module.

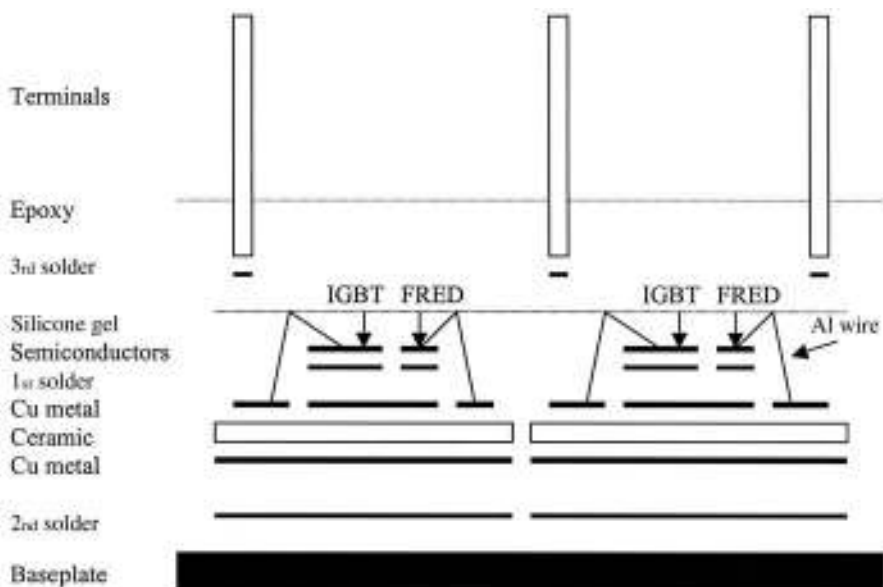


FIGURE 1.1
Structure of an IGBT power module.

Selection is based on the thermal, electrical, mechanical, and chemical properties of the materials. To these one must also add the elements of cost and degree of maturity. These are often the determining factors in the final selection of materials.

By adding control circuitry, the basic power module can be converted into an intelligent power module (IPM). A typical IPM consists of two sections:

- **Power section** (Figure 1.1) — With semiconductor components that provide the power for switching high-current and high-voltage load
- **Control (or intelligent) section** — With low-voltage, low-power ASIC components, which provide the control for gate drive, thermal shutdown, short-circuit protection, etc.

The power section is assembled using hybrid microelectronics technology on an expansive metallized ceramic substrate and a metal base plate. In order to reduce cost and to avoid heat-generating, high-temperature power components, the control section is usually built on a separate substrate (such as low-cost PCB), using standard surface-mount technology. The integration of these two sections is then performed, using one of the following two approaches:

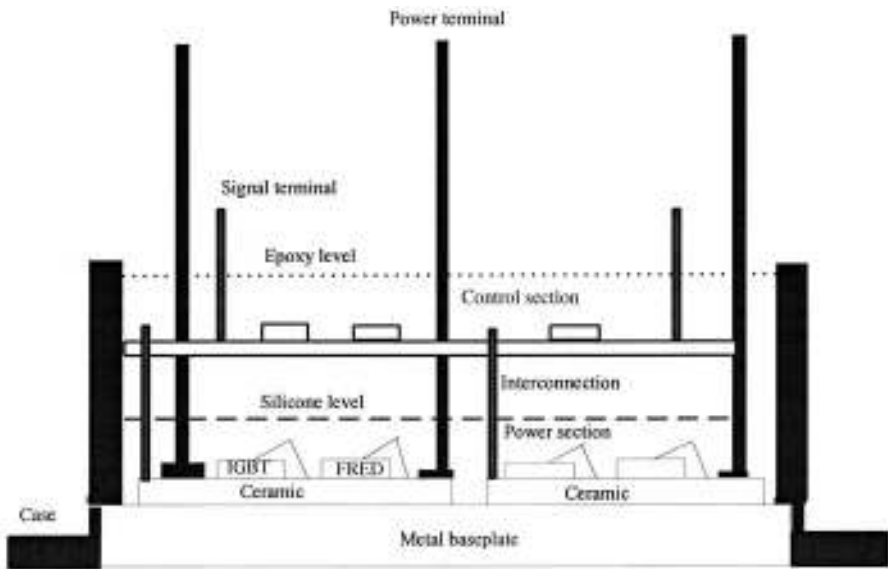


FIGURE 1.2
Conventional two-level power module.

- **Conventional approach**^{1,2} (Figure 1.2) — This is a single power module (30 mm in height) accommodating two or more separate levels: the power section occupies the lower level next to the heat sink, and the control section is on the upper level. The two levels are connected by electrical terminals.
- **Econo-pack approach**^{3,4} (Figure 1.3) — This is a low-profile package (12 mm in height) containing only the power section with pins provided on the exterior for connection to the PCB of the control section.

Production techniques for assembling these two sections are the same in either approach. The control section is application specific and varies greatly with usage. The power section, on the other hand, with standard circuit configurations and a series of voltage/current ratings, forms the fundamental building block of power conversion. The cost of the power module is primarily in the power section.

This book focuses on the design and manufacture of the power section (or simply the basic power module).

The contents are divided into these three main topics:

- **Chapter 3 — Materials**
- **Chapter 4 — Manufacturing processes and quality control**
- **Chapter 5 — Design and results**

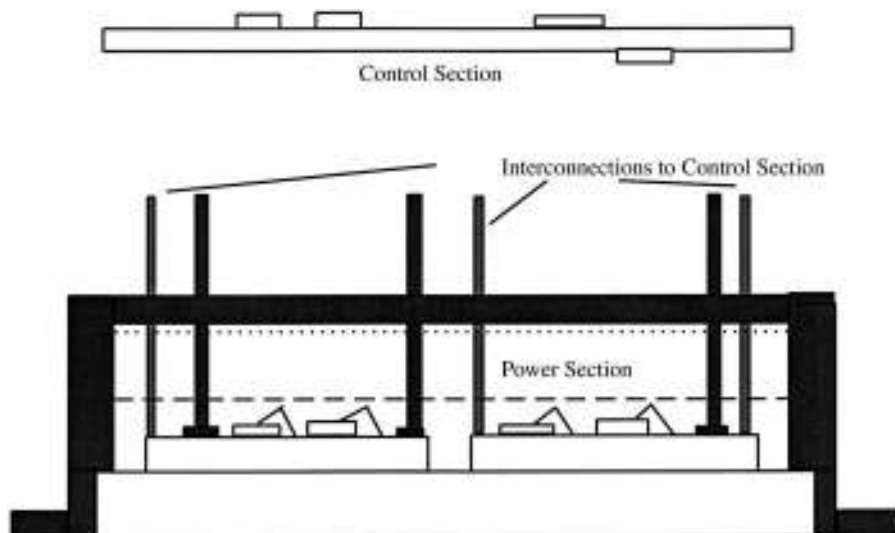


FIGURE 1.3
Econo-pack power module.

In [Chapter 3](#), the discussion centers on the materials used and their key properties — specifically electrical, mechanical, thermal, and chemical — presented in detailed table format. The materials here include both the popular old workhorses and the latest developments. (In solder, for example, one has the workhorse 63Sn/37Pb vs. the latest Pb-free 96Sn/3.5Ag/0.5Cu.) Materials' properties are compared with a list of criteria established as necessary requirements for the building of a high-performance, high-quality, and cost-effective power module. Selections are made. Pros and cons of each selection are analyzed. Some of these selections may be of interest to OEMs because they have the potential to offer a superior product to those currently available in the same market.

In [Chapter 4](#), the discussion shifts to manufacturing processes and quality control. An overview of the key manufacturing processes used by most IGBT module OEMs is presented. These include:

- IGBT chip sorting/grouping
- Cleaning technology
- Soldering
- Al wire bonding/solder bumping
- Electrical, thermal-electrical, and thermal-mechanical testing

These are mature but dynamic technologies. This overview not only covers the fundamentals but also attempts to include as many of the latest advances in these areas as possible. In addition, an innovative all-solder approach is

described. This new approach may be of interest to OEMs, due to its superior performance in certain characteristics.

Next, the subject of quality control is dealt with in two parts:

- **Process control** — Advanced inspection techniques, powerful tools, SPC, etc.
- **Long-term reliability** — DFR, HALT/HASS, failure analysis

Each key manufacturing operation and its corresponding inspection techniques are outlined. Inspection sites are positioned strategically along the production line to monitor the processes. Advanced techniques and powerful tools are required to provide valuable data on both the macroscopic and the microscopic levels. Examples are nondestructive thermal-mechanical characterization of the module stack, cleanliness of the surface, and SAM inspection of the solder attachments. These and other data can be displayed statistically.

The modules are designed for reliability (DFR) based on good design practices, promoting high performance and reliability. The finished modules are screened for infant mortality and life-tested for long-term reliability. Here, the screens are performed using HASS (highly accelerated stress screen) techniques. The life-tests rely on the concept of logarithmic time compression, designed to determine whether the modules still meet the long-term reliability goal established during the design phase, when HALT (highly accelerated life testing) was performed. Failure analyses are carried out and corrective action is implemented promptly to maintain the high level of reliability.

[Chapter 4](#) ends with two detailed manufacturing flow charts: one for the standard approach and one for the all-solder approach.

All pertinent information about such modules (manufacturing lot and date, electrical and thermal characteristics) can be stored in a barcode or in a 2D data matrix symbol, which is attached as a label to the case. With a simple scan, the user will have the complete “biography” of the module.

Finally, in [Chapter 5](#) the design of a power IGBT is presented, using the 200 A, 1200 V dual module in a half-bridge configuration as the vehicle. This is a three-step process. The first step is thermal management, in which thermal analyses on conduction and stress are performed on proposed stack structures. The next two steps deal with the physical layout of the module: [step 2](#) deals with circuit partitioning and [step 3](#) with design guidelines and considerations. Four different sample groups are built, based on the materials and processes presented in [Chapter 3](#) and Chapter 4 and by following the manufacturing flow charts outlined in Chapter 5. The characteristics of these samples are analyzed and compared. Detailed measured data are presented in the expectation that they may serve as useful design aids.

Although this book focuses on the design and manufacture of power IGBT modules, most of the discussions and results are general enough to be applicable to other types of power semiconductor modules as well.

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Selection Procedure

The following factors must be considered during the selection process:

- Thermal
- Electrical
- Mechanical
- Chemical
- Cost
- Maturity

The thermal factor plays the key role, due to the following issues:

Thermal stress — During a thermal fatigue or a temperature-cycling environmental test, each material tends to expand and contract according to its own coefficient of thermal expansion (CTE). Because the materials are all bonded together, each will exert thermal stress on the others. Any stress in excess of the material's mechanical strength will result in cracks.

Thermal conduction — During operation, the power semiconductor chips generate heat that must be removed effectively through the substrate/base-plate assembly so that the junction temperature of the power chips will stay within the desired level. The lower the junction temperature, the more reliably the module will function. The rate of failure mechanisms accelerates as temperature increases, roughly double for every 9°C rise. The module must therefore be properly thermally managed.¹⁻⁵

The selection of materials is an iterative process. A list of thermal, electrical, mechanical, and chemical requirements for each part is generated based on the following factors:

- Theoretical analysis
- Product analysis from different suppliers
- Published information
- Past experience

Under each category of material, the commonly used and the latest types are listed in relation to their thermal, electrical, mechanical, and chemical properties and to their maturity and cost. From these lists, a group of materials is selected that satisfies all or most of the established requirements. Thermal analyses on stress and conduction are performed on the theoretical stack of [Figure 1.1](#). The selections are adjusted until the calculated stress and the temperature rise are within the desired level. Figure 2.1 illustrates this procedure. The different stack designs in [Chapter 5](#) are based on this approach.

SELECTION OF MATERIAL

(Substrate, metallization, base plate, semiconductor chips, bonding material)

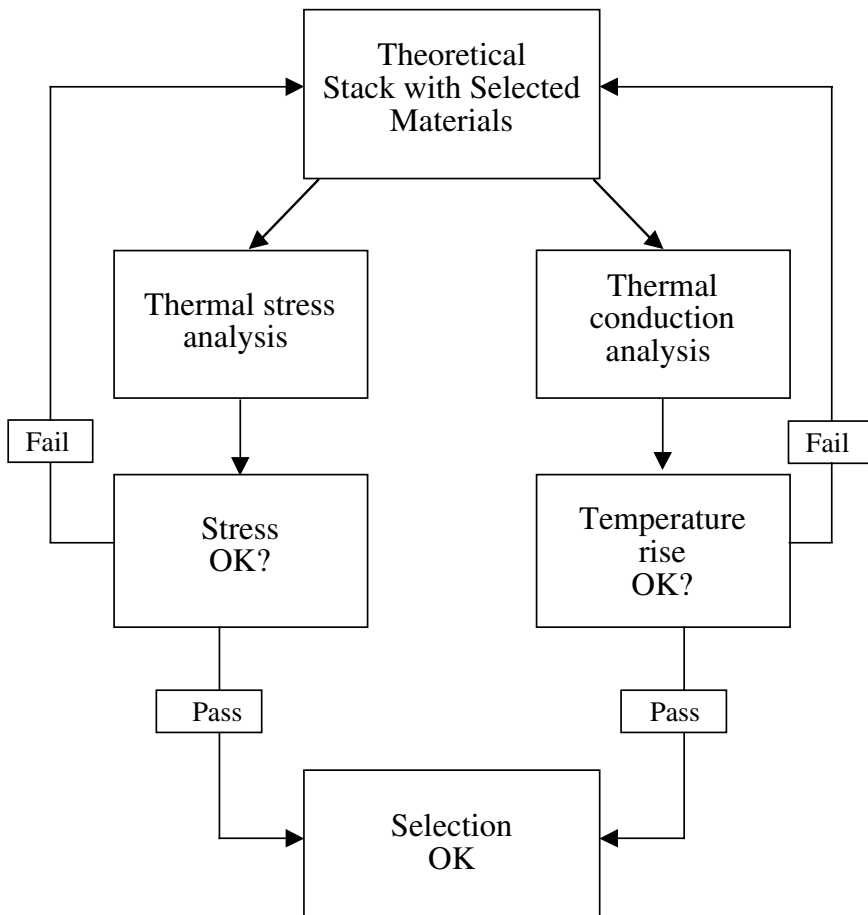


FIGURE 2.1

Selection of material (substrate, metallization, baseplate, semiconductor chips, bonding material).

References

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3. Licari, J.L. and Enlow, L.R., *Hybrid Microcircuit Technology Handbook*, 2nd edition, Noyes Publishing, Park Ridge, NJ, 1998.
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3.1 Insulating Substrate and Metallization

The insulating substrate serves as the supporting structure for the circuitry of the power module.¹ It acts as the surface for depositing conductive, dielectric, and resistive materials that form the passive circuit elements. It is also a base for mechanical support for all active and passive chip components. It must be strong enough to withstand different environmental stresses. Electrically, it must be an insulator to isolate various conductive paths of the circuit. It must be able to withstand an RMS AC voltage (50 to 60 Hz) of 2500 V applied between any terminal and the case, including the base plate, for a one-minute duration. It must have sufficient thermal conductivity to remove the heat generated by the components.

In addition, a high degree of surface smoothness is required for adhesion of films, fine conductor lines, and spacings. Surface flatness is desirable to minimize processing problems during screen-printing, photomasking, etc. Nonflat surfaces do not press uniformly against the base plate. This can potentially lead to microcracks and poor localized thermal conduction.

3.1.1 Selection Criteria

The substrate material most suitable for power applications should be determined by the following electrical, thermal, mechanical, and chemical requirements:^{2,3}

- Electrical
 - High-volume (or insulating) resistivity ($> 10^{12} \Omega \text{ cm}$)
 - High dielectric strength ($> 200 \text{ v/mil}$)
 - Low dielectric constant (< 15)

- Thermal
 - High thermal conductivity ($> 30 \text{ W/mK}$ for effective thermal conduction)
 - Matching coefficient of thermal expansion with the power semiconductor chips (2 to 6 ppm/ $^{\circ}\text{C}$ for minimizing thermal stress and matching with Si 2.8 ppm/ $^{\circ}\text{C}$)
 - High thermal stability ($> 1000^{\circ}\text{C}$ for direct bonded copper [DBC] and brazing operations)
- Mechanical
 - High tensile strength ($> 200 \text{ MPa}$)
 - High flexural strength ($> 200 \text{ MPa}$)
 - Dimensional stability — Hardness
 - Machineable — Can easily lap, polish, cut, and drill
 - Good surface finish ($< 1 \mu\text{m}$) — If not as fired, then should be able to be lapped to this specification
 - Metallizability — Compatible with popular metallization techniques:
 - Thin film
 - Thick film
 - Plated copper
 - Direct bonded copper (DBC)
 - Active brazed copper (ABC)
 - Regular brazed copper (RBC)
- Chemical
 - High resistance against acidic, alkaline, and other processing solvents
 - Low moisture absorption rate
 - Low toxicity
 - Chemically inert to plasma process
- Density/weight
 - Low density/weight — Minimize mechanical shock
- Maturity
 - Technology
 - Suppliers
- Cost
 - As close to that of alumina as possible

3.1.2 List of Insulating Substrates

Numerous insulating substrates of different materials have been used for semiconductor applications.²⁻⁴ The following is a list of the popular ones, grouped by type:

- Ceramic substrates
 - Alumina (Al_2O_3 : 96%, 99%)
 - Aluminum nitride (AlN)
 - Beryllia (BeO)
 - Boron nitride (BN, hex)
 - Cordierite
 - Fordterite
 - Mullite
 - Steatite
 - Titanate
- Glass substrate
 - Borosilicate glass
- Sapphire substrate
 - Sapphire
- Quartz substrate
 - Quartz
- Si-based substrates
 - SiC
 - SiO_2
 - Si_3N_4
- Metal-core substrates
 - Insulated metal substrates (IMS)
- Diamond substrate
 - Diamond (CVD polycrystalline)

Table 3.1 through Table 3.5 show the following properties of these insulating substrates:¹⁻²⁰

- Mechanical
- Thermal
- Electrical
- Chemical
- Other

TABLE 3.1

Mechanical Properties of Insulating Substrates

Material	Tensile Strength (MPa)	Flexural Strength (MPa)	Elastic Modulus (GPa)	Hardness	Surface Finish (μm)	Density (kg/m^3)
<i>Ceramic</i>						
Al_2O_3 (96%)	127.4	317	310.3	2000 K	1.0	3970
Al_2O_3 (99%)	206.9	345	345	9 MH	1.0	3970
AlN	310	360	310	1200 K	1.0	3260
BeO	230	250	345	100 K	15	3000
BN (hex)		110				2200
Corderite	55	10	14			1600
Forsterite	55	124	90			2700
Mullite		125	175			
Steatite	55	110	90			2500
Titanate	28	69	69			3500
<i>Glass</i>						
Borosilicate		50	9		1.0	2280
<i>Sapphire</i>						
Sapphire	399		430	9 MH	1.0	3990
<i>Quartz</i>						
Quartz	48	140	72	5 MH	1.0	2200
<i>Si-based</i>						
SiC	17	440	412			3160
SiO_2	96	30	69			2190
Si_3N_4	96	932	314			2400
<i>Metal-core</i>						
IMS	392	6				2700
<i>Diamond</i>						
Diamond (CVD)		1000	1180	7500 K	< 1.0	3500

Note: MH = Moh; K = Knoop.

TABLE 3.2

Thermal Properties of Insulating Substrates

Material	Thermal Conductivity (W/m °K)	CTE (ppm/°C)	Heat Capacity (J/kg-°C)	Maximum Use Temperature (°C)	Melting Point (°C)
<i>Ceramic</i>					
Al ₂ O ₃ (96%)	24	6.0	765	1600	2323
Al ₂ O ₃ (99%)	33	7.2	765	1600	2323
AlN	150–180	4.6	745	> 1000	2677
BeO	270	7.0	1047		2725
BN (hex)	60	3.8			
Corderite	4	3.0	770	1250	
Forsterite	4	11		1100	
Mullite	6	4.2			
Steatite	2.5	10.5		1100	
Titanate	4	10	700		
<i>Glass</i>					
Borosilicate	2	3.2			
<i>Sapphire</i>					
Sapphire	41.7	7.3	735		
<i>Quartz</i>					
Quartz	43	5.5	816	1140	1938
<i>Si-based</i>					
SiC	120	4.6	675	> 1000	3100
SiO ₂	1.5	0.6		> 800	
Si ₃ N ₄	70	3.0	691	> 1000	2173
<i>Metal-core</i>					
IMS	4	25			
<i>Diamond</i>					
Diamond (CVD)	2000 (Z) 1400 (X,Y)	1	509	Resistant to oxidation to 600°C	

TABLE 3.3

Electrical Properties of Insulating Substrates

Material	Resistivity ($\Omega\text{-cm}$)	Dielectric Strength (kV/mm)	Dielectric Constant at 1 MHz
<i>Ceramic</i>			
Al ₂ O ₃ (96%)	$> 10^{14}$	12	9.2
Al ₂ O ₃ (99%)	$> 10^{14}$	12	9.9
AlN	$> 10^{14}$	15	8.9
BeO	$> 10^{14}$	12	6.7
BN (hex)			4.1
Corderite	$10^6\text{--}10^{14}$		
Forsterite	$10^{10}\text{--}10^{12}$	7.9–11.8	6.2
Mullite	$> 10^{12}$		
Steatite	$10^{11}\text{--}10^{13}$	7.9–15.7	5.5–7.5
Titanate	$10^6\text{--}10^{13}$	2.0–11.8	15
<i>Glass</i>			
Borosilicate	$> 10^{14}$		3.7
<i>Sapphire</i>			
Sapphire	$> 10^{14}$	48	10.4
<i>Quartz</i>			
Quartz	10^{10}	16.1	3.8
<i>Si-based</i>			
SiC	$> 10^{11}$		20–42
SiO ₂	$> 10^{14}$		3.5–4
Si ₃ N ₄	$> 10^{10}$	10	6–10
<i>Metal-core</i>			
IMS	$> 10^{13}$		
<i>Diamond</i>			
Diamond (CVD)	$> 10^{11}$	> 100	5.7

TABLE 3.4

Chemical Properties of Insulating Substrates

Material	Moisture Absorption (%)	Nitric Acid	Sulfuric Acid (Weight Loss at mg/cm ² /day)	Caustic Soda	Toxicity
<i>Ceramics</i>					
Al ₂ O ₃ (96%)	0				No
Al ₂ O ₃ (99%)	0	0.05	0.22	0.04	No
AlN	0				No
BeO	0				Yes
BN (hex)	0				No
Corderite	27				No
Forsterite	0				No
Mullite	5–15				No
Steatite	0				No
Titanate	0				No
<i>Glass</i>					
Borosilicate	0				No
<i>Sapphire</i>					
Sapphire	0	0	0	0	No
<i>Quartz</i>					
Quartz	0	0	0	0	No
<i>Si-based</i>					
SiC	0	0.04	0.01	0	No
SiO ₂	0				No
Si ₃ N ₄	0	1.00	0.40	0.36	No
<i>Metal-core</i>					
IMS	0				No
<i>Diamond</i>					
Diamond (CVD)	0	0	0	0	No

TABLE 3.5**Other Properties of Insulating Substrates**

Material	Metallizability^a	Machineability^b	Relative Cost
<i>Ceramics</i>			
Al ₂ O ₃ (96%)	All, except thin film	Good	1×
Al ₂ O ₃ (99%)	All	Good	2×
AlN	All, except thick film	Good	4×
BeO	All	Good (only by approved source)	5×
BN (hex)	None	Good	
Corderite	Thick film	Good	0.6×
Forsterite	Thick film	Good	1×
Mullite	Thick film	Good	1×
Steatite	Thick film	Good	0.8×
Titanate	Thick film	Good	2×
<i>Glass</i>			
Borosilicate	Thin film	Fair	1×
<i>Sapphire</i>			
Sapphire	Thin film	Fair	10×
<i>Quartz</i>			
Quartz	Thin film	Fair	8×
<i>Si-based</i>			
SiC	None	Fair	4×
SiO ₂		Good	
Si ₃ N ₄	All	Good	2.5×
<i>Metal-core</i>			
IMS	Thin and thick films	Good	
<i>Diamond</i>			
Diamond (CVD)	Thin and thick films	Good	High

^a Metallization: Thin film, thick film, plated copper, direct bonded copper (DBC), active brazed copper (ABC), regular brazed copper (RBC).

^b Machineability: lapping, polishing, cutting, drilling, shaping.

3.1.3 Selected Insulating Substrates

After carefully examining the preceding tables and comparing them with the selection criteria, it appears that there are four possible candidates for insulating material that are suitable for power semiconductor applications:

- Ceramic substrates:
 - Al_2O_3 (96%, 99%)
 - AlN
 - BeO
- Si-based substrate:
 - Si_3N_4

CVD polycrystalline diamond substrate has promising potential if:

- Heavy Cu metallization can be attached
- Cost can be reduced

In the following sections, the strengths and weaknesses of each of these substrates are analyzed and compared.

3.1.3.1 Alumina (96%, 99%)

- Strengths:
 - Most commonly used ceramic for substrate material and therefore the most mature technology
 - Low cost — 1" × 1" size as fired, 96% ~ \$0.10; 99% ~ \$0.20
 - Average but adequate all-around characteristics: mechanical, thermal, electrical, and chemical
 - Easily metallized — thin film, thick film, plated copper, DBC, ABC, RBC
 - Easily machineable
 - Nontoxic
 - Nonpermeable to gas
 - Zero moisture absorption rate
 - Camber ~ 0.003"/1"
 - Mature technology
 - Dimensionally stable

- Weaknesses:
 - Thermal conductivity ~ 30 w/k-m is adequate for low- to medium-power applications but ineffective for high power. For example, a 25-mil thick substrate with 10 mils of Cu on both sides and a $0.4'' \times 0.4''$ IGBT chip attached to it has a thermal resistance of about 0.30 w/k-m. This means that for an acceptable T_j rise of 30°C , the IGBT chip can only operate at 30 to 40A. This chip is rated at about 75A and so is greatly underutilized.
 - Thermal expansion mismatch with Si — 6.0 to 7.2 ppm/ $^\circ\text{C}$ for Al_2O_3 vs. 2.8 ppm/ $^\circ\text{C}$ for Si.
 - High dielectric constant.
 - Average chemical resistance ability against acid.
- Comments:
 - More appropriate for low- to medium-power applications.
 - High-volume and low-cost applications.
 - Good material for hermetic packages.
 - For power applications, 99% Al_2O_3 is a better compromise between cost and performance than the 96%.
 - If cost is an issue in the high-power application, then a very thin Al_2O_3 (10 mil) with 8 mils of Cu on both sides may be considered as an alternative. In this case, the small thickness will compensate for the low thermal conductivity of Al_2O_3 . The trade-offs are in the isolation voltage, V_{ISO} , and in mechanical fragility.

3.1.3.2 Aluminum Nitride (AlN)

- Strengths:
 - Very good thermal conductivity — Six times that of Al_2O_3
 - Very effective for high-power semiconductor applications
 - Good thermal expansion matching with Si — 4.6 ppm/ $^\circ\text{C}$ for AlN vs. 2.8 ppm/ $^\circ\text{C}$ for Si
 - Mechanical, thermal, and all other electrical characteristics are average but adequate (comparable to those of Al_2O_3)
 - Easily machineable
 - Nontoxic
 - Nonpermeable to gas
 - Zero moisture absorption rate
 - Inert to most chemicals
 - Camber $\sim 0.003''/1''$
 - Dimensionally stable

- Weaknesses:
 - Relatively new material, so its technology is not as mature as Al_2O_3 and beryllia.
 - DBC metallization on AlN has difficulties. Thermal fatigue failure is a major concern for DBC AlN substrate.
 - Thick-film metallization process is not as repeatable and reliable as Al_2O_3 .
 - Four times more expensive than Al_2O_3 .
 - Poor resistance against alkaline environment — Requires special cleaning agent.
 - May decompose into hydrated alumina in the presence of high temperature and humidity.
- Comments:
 - One of the best all-around substrate materials for high-power semiconductor applications.
 - Due to its average mechanical fracture strength, it is preferred to be used in conjunction with a metal base plate. Otherwise, substrate thickness must be about 80 mils if it is exposed directly to external environment without a metal base plate.
 - Thermal fatigue capabilities depend very much on the following:
 - Bonding technique of Cu foil to the AlN substrate
 - Design of the Cu foil
 - Substrate thickness
- Particular care must be exercised in selecting the right vendors.

3.1.3.3 *Beryllia (BeO)*

- Strengths:
 - Excellent thermal conductivity — Eight times that of Al_2O_3
 - Very effective for high-power semiconductor applications
 - Mature technology
 - Thermal, electrical, and all other chemical characteristics are average, but adequate (comparable to those of Al_2O_3)
 - Easily metallized — Thin film, thick film, plated copper, DBC, ABC, and RBC
 - Nonpermeable to gas
 - Zero moisture absorption rate
 - Mature technology
 - Dimensionally stable

- Weaknesses:
 - Toxic in both powder and vapor form:
 - Machining, such as cutting, drilling, and shaping, must be handled only by specialty vendors
 - Environmental issues are a major concern when disposing of the material
 - Limited suppliers
 - Thermal expansion mismatch with Si — 7.0 ppm/°C for BeO vs. 2.8 ppm/°C for Si
 - Mechanical characteristics are below average, with mechanical strength only 60% that of Al₂O₃
 - Five times more expensive than Al₂O₃
- Comments:
 - Used by the defense industry
 - For power semiconductor applications where thermal management consideration cannot be served in any other way

3.1.3.4 *Silicon Nitride (Si₃N₄) — Sintered*

- Strengths:
 - Excellent thermal expansion match with Si — 3.0 ppm/°C for Si₃N₄ vs. 2.8 ppm/°C for Si
 - Very strong mechanically:
 - Mechanical fractural toughness is more than double those of Al₂O₃ and AlN, and triple that of BeO
 - Good thermal conductivity — Two-and-a-half times that of Al₂O₃
 - Effective for high-power semiconductor applications
 - Thermal and all other electrical characteristics are average but adequate (comparable to those of Al₂O₃).
 - Easily metallized — Thin film, thick film, plated copper, DBC, ABC, RBC
 - Easily machineable
 - Nontoxic
 - Nonpermeable to gas
 - Zero moisture absorption rate
 - Creep resistance
 - Good high-temperature strength
 - Good thermal shock resistance
 - Dimensionally stable

- Weaknesses:
 - New material with relatively immature technology — Use of this material in the power semiconductor field is in the infancy stage.
 - Limited suppliers.
 - Weak chemical resistance against acidic environment.
 - Two to two-and-a-half times more expensive than Al_2O_3 .
- Comments:
 - Price will come down as usage increases.
 - Si_3N_4 is probably the best material to be used as a stand-alone substrate* (no metal base plate) for high-power semiconductor applications. It is also conceivable that power semiconductor chips can be attached to the top side of the substrate, with the bottom side having a finlike structure† formed or machined for the purpose of heat dissipation. In this way, the heat sink can be integrated directly with the substrate without the use of any mechanical force or thermal interface material.²¹
 - Good for applications where thermal fatigue capability is highly desired.

Table 3.6 presents a list of suppliers for ceramic substrates.

TABLE 3.6

List of Substrate Suppliers

Supplier	96% Al_2O_3	99% Al_2O_3	AlN	BeO	Si_3N_4
Brush Wellman	X	X		X	
Carborundum	X	X	X		
Ceradyne	X	X		X	X
CeramTec	X	X	X		
Coors	X	X		X	
Curamik	X	X	X		
Denka	X	X	X		X
Insaco	X	X			
Kyocera	X	X	X		X
Lambertville	X	X			
NGK	X	X			X
Stellar			X	X	
Wesgo (Morgan Advanced Ceramics)	X	X	X		X

* Patent pending.

† Patent pending.

3.1.4 Metallization on Insulating Substrates

For power semiconductor applications, the metallizations on the insulating substrates should possess the following characteristics:^{1,2,3,5,12,13}

- Thermal:
 - High thermal conductivity ($> 200 \text{ w/k-m}$)
 - Matching thermal expansion with insulating substrate
 - High thermal fatigue capability — Greater than 1000 cycles from -40 to 100°C with no failures at the interface with the substrate
 - High thermal stability — Greater than 1000°C in order to be compatible with the direct bonding and brazing operations
- Electrical:
 - Able to conduct high current density
 - Low electrical resistivity — Typically, ohmic drop across the metallization should not exceed one-tenth of the IGBT's V_{CESAT}
- Mechanical:
 - Strong adhesion to the substrate — High peeling strength
 - Al wire-bondable
 - Solderable for standard solder (such as 95Pb/5Sn, etc.)
 - Applicable to the previous four selected insulating substrates — Al_2O_3 , AlN, BeO, and Si_3N_4
 - Compatible with standard processing equipment
- Chemical:
 - Photoetchable — Designed pattern can be easily formed (for the case of thick film, this is not required)
 - High chemical resistance against standard processing solvents
 - Nontoxic
 - Good corrosion resistance
 - Chemically inert
- Cost:
 - Low

3.1.5 Types of Metallizations

3.1.5.1 Metallization Technologies

The insulating substrate is typically metallized by one of the methods listed in [Table 3.7](#).

TABLE 3.7
Metallization Technologies

Thick Film	Thin Film	Copper Metallization
Polymer	Sputtering	Plated copper
Cermet	Evaporation	Direct bonded copper
Gold	Gold	Active brazed copper
Silver	Silver	Regular brazed copper
Copper	Copper	
Palladium silver	Aluminum	
Platinum gold		
Platinum silver		
Refractory		
Tungsten		
Molybdenum		
Moly-manganese		

3.1.5.2 *Types of Metallization*^{2,3}

3.1.5.2.1 *Thick Film*

Thick-film circuits are typically fabricated by screen-printing a specially formulated paste onto a substrate, which is dried and then fired at high temperature. The paste can be in the form of a conductor, resistor, capacitor, inductor, fuse, varistor, transient voltage suppressor, or thermistor. Typical film thickness is from 0.5 to 2.0 mils.

There are three basic categories of thick film:

- Polymer
- Cermet
- Refractory

3.1.5.2.1.1 *Polymer* — Polymer thick film (PTF) is a polymeric resin mixed with conductive, resistive, or insulating particles. It is fired or cured at temperatures ranging from 85 to 300°C, typically from 120 to 165°C. It is low in cost, limited to low-temperature operation, and widely used in plastic or organic substrates.

3.1.5.2.1.2 *Cermet* — This is the most popular type and is applicable to both ceramic and Si-based substrates.

It consists of a mixture of the following:

- Active element — To establish the function of the film
- Adhesion element — To provide adhesion to the substrate
- Organic binder — To provide proper fluid properties for screen printing
- Solvent or thinner — To adjust the viscosity

This mixture is fired at a range from 850 to 1000°C.

TABLE 3.8

Popular Thick Film Materials

Material	Resistively, ρ (m Ω /□)
Gold	3
Silver	1
Copper	2
Palladium silver	30
Palladium gold	50
Platinum gold	50

The adhesion of the thick film to the substrate is above average, and the thermal fatigue capability is rated as fair.

Popular thick film materials are shown in Table 3.8.

The maximum current allowed for each type of material can be calculated from the following:

- Cross-sectional area of the metallization
- Maximum power dissipation allowed for each material

For example:

- Al₂O₃ substrate — 4 watt/cm²
- BeO substrate — 80 watt/cm²
- AlN and Si₃N₄ substrates are somewhere in between

Because the typical thick-film thickness is 0.5 mil or 12 μ m, it can be seen that the maximum current-carrying capability is about a few amperes.

3.1.5.2.1.3 Refractory — These are special kinds of cermet thick film that can withstand high-temperature operations. They are typically fired at a much higher temperature (1500 to 1600°C) in a reducing atmosphere. The adhesion of these films to the substrates is strong, and the thermal fatigue capability is rated as very good. Popular refractory materials are tungsten and molybdenum (Table 3.9).

The maximum current carrying capability is limited to 1 to 2 amperes for these materials.

TABLE 3.9

Popular Refractory Materials

Refractory Material	Resistively, ρ (m Ω /□)
Tungsten	22–32
Molybdenum	15

3.1.5.2.2 *Thin Film*

Thin-film circuits are typically fabricated by first sputtering or evaporating the film across the entire surface of the substrate. This film is then coated, photoprocessed, and etched to form the desired pattern. Thin film offers better definition and narrower lines than thick film. It is most suitable for high-density and high-frequency applications. Thin film metallization adheres strongly to the substrate and provides excellent thermal fatigue performance. Wire bondability is also superior to that of thick film.

Due to the labor and specialty equipment involved, thin-film circuits are almost five to six times more expensive than thick film. Also, multilayer thin-film structure is extremely difficult and expensive to fabricate. Popular thin-film materials include the following:

- Gold
- Silver
- Copper
- Aluminum

Typical thickness is about 0.1 mil (2.5 μm) or less. Current-carrying capability is limited to a few amperes.

3.1.5.2.3 *Copper Metallization*

Both thick-film and thin-film technologies are limited in their thickness, usually to less than 1 mil (25 μm). This limitation affects their ability to conduct large currents.

Copper metallization technology provides three features:

- Increased metallization thickness
- Improved current-carrying capability
- Improved thermal spreading

Four basic techniques are available:

- Plated copper
- Direct bonded copper (DBC)
- Active brazed copper (ABC)
- Regular brazed copper (RBC)

However, as the copper metallization thickness increases, its thermal expansion mismatch with the insulating substrates becomes more and more pronounced, as shown in [Table 3.10](#).

This large mismatch will be manifested during thermal fatigue tests, which can potentially lead to excessive thermal stress and eventually to micro-cracks. Proper metallization design and processing techniques must be

TABLE 3.10

CTE of Insulating Substrates and Copper Metallization

Material	CTE (ppm/°C)
Al ₂ O ₃ (96%)	6.0
Al ₂ O ₃ (99%)	7.2
AlN	4.6
BeO	7.0
Si ₃ N ₄	3.0
Cu	17.0

utilized to minimize or eliminate these cracks. This requires careful screening of suppliers.

Copper has the additional problems of adhesion and being very chemically reactive. A barrier layer is required to improve adhesion, and a Ni or Au layer is required on the surface for protection.

3.1.5.2.3.1 Plated Copper — The concept behind this technique is to build up the thickness of copper material by electroplating. A film is first deposited onto the substrate, either by a thin-film method (sputtering or evaporation) or a thick-film process (screen-printing). Typical materials used are Moly/Mn for thin film and copper for thick film. A layer of electroless copper may be plated over this film surface, followed by electrolytic copper to increase the thickness. The plated copper film is then fired at an elevated temperature in a nitrogen atmosphere to improve adhesion. The thermal fatigue strength of plated copper is rated as good. One supplier has successfully performed 1000 cycles from -55 to 150°C without failure for 4-mil thick plated Cu.

Maximum copper thickness achievable after electroplating is about 5 to 8 mils, with density of about 70% of regular copper material. Fine patterns can be generated by photolithographic etchings. For thicker film, this may result in undercutting and loss of resolution. Current-carrying capability has been reported up to 50 A.

3.1.5.2.3.2 Direct Bonded Copper^{3,17,18} — This technique uses a high-temperature process to achieve an intimate bond between the copper and the ceramic. There is no solder or any other catalyst used in the interface between the copper and the ceramic surface. Here, the combination of copper and ceramic is heated to a temperature of about 1070°C, slightly below copper's melting point, in a nitrogen atmosphere. At this temperature, the copper oxide forms a eutectic melt that wets and, when cool, produces a strong bond between copper and ceramic.

Copper thickness is typically 8 to 20 mils, and patterns can be formed by photolithographic etching. Fine resolution is difficult due to undercutting. Minimum line width and separation are 20 mils. Copper is usually bonded to both surfaces of the substrate in order to balance thermal expansion.

Because a layer of copper oxide is required for the direct bonding process, AlN and Si₃N₄ ceramics must be treated first in order to apply this technique. This involves an additional oxidation process at about 125°C. However, this added oxygen diffuses along grain boundaries and may downgrade the thermal conductivity of AlN and Si₃N₄.

Direct bonded copper offers the following advantages for power packaging:

- The copper and ceramic tend to act, often bonding, like an integral unit with a single coefficient of thermal expansion. This coefficient is much lower than that of pure copper and more closely matched to that of the ceramic. It is therefore possible to solder even large chips directly onto the copper layer without risking stress damages.
- The copper used is of the high-purity, oxygen-free high-conductivity (OFHC) type. With proper line width and thickness, the metallization can be of very low electrical resistance and can handle current well in excess of 100 A.
- The thick layer of copper provides efficient heat spreading from the power chips.

3.1.5.2.3.3 Active Brazed Copper — The active brazed copper process utilizes brazing alloy to form a bonding layer between copper and ceramics.^{3,16} An example is the alloy of silver, copper, titanium, and zirconium in the ratio 72Ag/28Cu/3TiH₂/3Zr.

The braze is usually applied in the form of a paste. Most suppliers use the screen-printing technique. The resulting titanium braze layer provides superior adhesion and thermal cycle performance.

Active brazed copper has been applied extensively to AlN and lately to Si₃N₄ substrates, where DBC techniques have experienced difficulties. During direct bonding operation on these ceramics, oxygen gas must be fed into the critical interface region. This added oxygen will diffuse along grains and reduce the thermal conductivity of the ceramics. Furthermore, the release of gases during the direct bonding process may require a perforated Cu foil design. However, this results in a loss of conduction area for current. The advantages of using the ABC process over DBC for these two substrates are as follows:

- Better adhesion
- Better current-carrying capability
- Better thermal-fatigue capability

3.1.5.2.3.4 Regular Brazed Copper — The technique is similar to that of the active brazed copper, except that it is performed in a vacuum. In this case, typically a thin silver film is first sputtered onto the substrate. Ag-braze alloy is then applied to the film in the form of a paste, and the copper foil is placed

TABLE 3.11

Metallization for Different Insulating Substrates

Technology	Al ₂ O ₃	AlN	BeO	Si ₃ N ₄
Thin film	Good	Good	Good	Good
Thick film	Good	Fair	Good	Fair
Plated copper	Good		Good	
DBC	Good		Good	
ABC		Good		Good
RBC		Good		Good

on top. The combination is then heated to the melting point of the braze alloy. After brazing, the top foil may be photoetched to form the desired pattern.

One supplier noted that the titanium-based brazing alloy is overly active and can potentially lead to nonuniform brazing. Regular Ag-based braze is more controllable and therefore results in a more uniform and stronger adhesion.

Table 3.11 and [Table 3.12](#) compare different metallizations available for the insulating substrates.

For a conductor of 40 mil width and 12 mil thickness on an Al₂O₃ substrate, the temperature rise for a 100 A operating current is about 17°C. From Table 3.11, we can conclude that the metallizations for high-power semiconductor applications are:

- Direct bonded copper (DBC)
- Active brazed copper (ABC)
- Regular brazed copper (RBC)
- Plated copper (possibly)

An estimate of the total cost of the insulating substrate per square inch with metallizations at thickness of 25 mils is as shown in [Table 3.13](#).

3.1.6 Analysis of Copper Metallization Suppliers

It should be noted that the preceding description of the technology is very general. Every supplier has its own unique processing features and design techniques that can affect performance, especially thermal fatigue and cost. [Table 3.14](#) through [Table 3.17](#) provide lists of suppliers and their capabilities. This information is gathered from publications, conferences, or private conversations.

TABLE 3.12Comparison of Metallization Technologies^{4,5}

Technology	Adhesion	Geometry	Process	Electrical	Thermal Fatigue	Process Cost
Thin film	Good	0.002 line < 0.005 thick	Good wire bondability; fair solderability	1–2 A	Good	High
Thick film	Fair	0.010 line > 0.005 thick	Good wire bondability; good solderability	2–5 A	Fair	Low
Plated copper	Fair	0.004 line 0.005 thick	Good wire bondability; good solderability	50 A	Fair	Medium
DBC	Good	0.020 line typ 0.020 thick	Good wire bondability; good solderability	> 200 A ^a	Good for Al ₂ O ₃ and BeO	Low
ABC, RBC	Good	0.020 line typ 0.020 thick	Good wire bondability; good solderability	> 200 A	Good for AlN and Si ₃ N ₄	Low

^a For a conductor of 40 mil width and 12 mil thickness on a Al₂O₃ substrate, the temperature rise for 100 Amp. operating current is about 17°C.

TABLE 3.13

Estimated Total Cost of Insulating Substrate per Square Inch

<i>Metallized Insulating Substrate</i>	<i>Cost per Square Inch</i>
Al ₂ O ₃ with DBC	\$1.00–\$1.50
Al ₂ O ₃ with plated copper	\$2.00–\$2.50
AlN with ABC (or RBC)	\$3.50–\$5.00
Si ₃ N ₄ with ABC	\$3.00–\$5.00

TABLE 3.14

Suppliers of Ceramic Substrate with Plated Copper Metallization

Supplier	Al ₂ O ₃	AlN	BeO	Si ₃ N ₄
<i>Plated Copper</i>				
1. Remtec	• 96% • 1–10 mil thick • 0.6–0.07 m/□ • Current up to 50 A • Pass 1000 cycles from –55 to 150°C for 4 mil Cu • Pass 1000 cycles from 0 to 70°C for 10 mil Cu • Wire bondability for Al and Au wire	• 99.5%	• 99.5% • 1–10 mil thick • 0.6–0.07 m/□ • Current up to 50 A • Wire bondability for Al and Au	
2. Zecal	• 96% • Up to 5 mil thick • 0.5 m/□ • No thermal fatigue data			
3. Tech-Ceram	• 96% • 1 mil of W • ~5 mils of Cu • Excellent thermal fatigue, no specific data		• 99.5% • 1 mil of W • ~5 mils of Cu • Excellent thermal fatigue, no specific data	
4. Thermic Edge ZiMarc		• 99.5% AlN • Up to 2 mil thick • 0.7 m/□ • Pass 10 cycles from –65 to 150°C		

TABLE 3.15

Suppliers of Ceramic Substrate with DBC Metallization

Supplier	Al ₂ O ₃	AlN	BeO	Si ₃ N ₄
<i>DBC</i>				
1. Stellar Ind.	• 96% • 25 mil substrate • 5, 8, 10, 12 mils Cu (Cu P/N : CPA110) • Pass 3000 cycles from -40 to 125°C for a 25 mil substrate with 10 mil Cu on both sides		• 99.5% • 25 mil substrate • 5, 8, 10, 12 mils Cu (Cu P/N : CPA110) • Pass 3000 cycles from -40 to 125°C for a 25 mil substrate with 10 mil Cu on both sides	
2. Brush Wellman	• 96% • 25, 40 mil substrate max. size 5.4" × 6.5" • 8, 10, 12 mil Cu (Cu P/N : CDA101,102 110) • Pass 1000 cycles from -65 to 125°C for a 40 mil substrate with 8 mil Cu on both sides		• 99.5% • 25, 40 mil substrate max. size 2" × 2" • 8, 10, 12 mil Cu (Cu P/N : CDA101,102,110)	
3. Curamik	• 96% • 10, 15, 25, 40 mil substrate max. size 5" × 7" • 8, 12, 16, 20 mil Cu • Pass 1000 cycles from -45 to 130°C for a 25 mil Al₂O₃ with 12 mil Cu both sides	• 99.9% AlN • 25, 40 mil substrate • 8, 12, 16 mil Cu • Pass 1000 cycles from -55 to 125°C for a 25 mil AlN with 12 mil Cu both sides (special Cu dimple design)		

TABLE 3.16

Suppliers of Ceramic Substrate with ABC Metallization

Supplier	Al ₂ O ₃	AlN	BeO	Si ₃ N ₄
<i>ABC</i>				
1. Denka		• 99.5% • 16, 25, 40, 80 mil substrate max. size 3.5" × 4" • 4–12 mil Cu • Braze: Ag/Cu/TiH₂/Zr • Pass 3000 cycles –40 to 125°C for a 25 mil substrate 12 mil Cu on top 6 mil Cu on bottom (use of shock absorption layer and special Cu metal design)		• 25 mil substrate max size 2.5" × 3.5" • 8–12 mil Cu • Braze: Ag/Cu/TiH₂/Zr • Pass 3000 cycles –40 to 125°C for a 25 mil substrate 12 mil Cu on top 6 mil Cu on bottom
2. Stellar Ind.		• 99.5% • Braze: Ti alloy • Pass 900 cycles from –55 to 125°C for a 25 mil AlN with 10 mil Cu on both sides (Cu P/N: CDA110)		
3. Thermic Edge ZiMarc		• 99.5% • 25, 40 mil substrate max. size 4" × 4" • 5, 8, 10, 12 mil Cu • Braze: Ti alloy • Pass 1000 cycles from –40 to 125°C for a 25 mil substrate with 10 mil Cu on top 5 mil Cu on bottom		

TABLE 3.17

Suppliers of Ceramic Substrate with ABC Metallization

Supplier	Al ₂ O ₃	AlN	BeO	Si ₃ N ₄
RBC				
Tech-Ceram		• 99.9% • Braze Cu onto Ag film using Ag/Cu alloy • Pass 1000 cycles –55 to 125°C for a 25 mil substrate with 10 mil Cu on both sides • Stronger than ABC		

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3.2 Baseplate

The baseplate serves as a mechanical support for the insulating substrate. It absorbs heat during power transients and transmits heat from the insulating substrate to the system's heat sinking coolant. It must be highly thermally conductive so as to dispose efficiently of the waste heat generated by the power devices. It must also have a high degree of surface smoothness so that there are no voids between it and the insulating substrate. Voids will cause hot spots that will eventually lead to cracking and poor reliability. Finally, it must provide a controlled and reproducible warpage that ensures intimate contact with the heat sink.

3.2.1 Selection Criteria

The baseplate material chosen for this power application must be compatible with the insulating substrate material and must meet the following thermal, mechanical, chemical, and other requirements:

- Thermal:
 - Thermal conductivity (W/mK) — Greater than 150
 - Coefficient of thermal expansion (CTE) — Compatible with the insulating substrate
- Mechanical:
 - High tensile strength — Greater than 200 Mpa (or 29 Ksi)
 - High flexural strength
 - Easily shaped and bent

- Good surface finish — Greater than 2 μm
- Chemical:
 - High resistance to processing solvents
 - Low moisture absorption rate
 - Low toxicity
- Density/weight:
 - Low density/weight — To minimize damage due to mechanical shock
- Cost:
 - As close to copper as possible:
 - Maturity of technology
 - Abundance of suppliers

3.2.2 List of Baseplate Materials

There are a large number of baseplate materials and configurations that are used in power electronics applications.^{1,2} Half-hardened OFHC copper continues to be the predominant choice. Most other high-performance base plates are fabricated using composite materials that vary not only with component percentages, but also with particle sizes of their constituent powders and the alloy components of their metals. So far, the state-of-the-art composites are mostly polymer, metal, and carbon matrices reinforced with fibers, particles, or both. The reinforcements come in the following forms:

- Continuous thermally conductive carbon fibers
- Discontinuous thermally conductive carbon fibers
- Thermally conductive ceramic (SiC, BeO) and diamond particles

Composites with fiber reinforcement are usually anisotropic, whereas those with particle reinforcement are isotropic.

The processing of composite materials is another variable that must be considered. Suppliers with similar component ratios have reported different results. The continued development of new composite materials should result in improved processes at reduced costs, helping improve continuously the cost and performance of the power module.

We will narrow the selection to baseplate materials that are compatible with the insulating substrate materials in [Section 3.1.3](#) of this chapter.

Because all the base-plate materials under consideration contain either aluminum or copper as the exposed element, they may require nickel or nickel/gold plating to enhance solderability and to protect them from corrosion.

These materials are under consideration for use as the baseplate material:¹⁻⁹

- Copper
- Aluminum
- Copper/molybdenum/copper laminate (CuMoCu)
- Aluminum/silicon carbide metal matrix (AlSiC)
- Copper/tungsten matrix (Cu/W)
- Copper/molybdenum matrix (Cu/Mo)
- Copper/graphite matrix
- Copper/diamond matrix (Dymalloy)
- Aluminum/graphite matrix

Of the preceding materials, only CuMoCu is macrocomposite; the rest are all microcomposites.

3.2.3 General Summary of Available Base Materials

Table 3.18 shows the range of thermal properties available for various materials that can be used as a baseplate.^{1,3-9}

Net-shape enables texturing the bottom surface with fins or bumps to increase the transfer area between the baseplate and the cooling liquid. In volume production, the net-shape process can eliminate the need for machining.

From Table 3.18, it appears that all have sufficient thermal conductivity characteristics. Aluminum-based materials give the most favorable density.

TABLE 3.18

General Properties of Available Base Materials

Material	Density (g/cm ³)	CTE (ppm/°C)	Thermal Conductivity (W/mK at 25°C)	Available Forms
Cu ^a	8.96	17.8	398	Sheet
Al	2.7	23.6	238	Sheet
Cu/Mo/Cu	9.36–10.02	5.1–8.6	166–311	Sheet
AlSiC	2.97–3.04	6.5–13.8	170–200	Net-shape
Cu/Mo	9.3–10	6.8–13	165–275	Sheet
Cu/W	14.8–17	5.6–9	130–205	Sheet, net-shape
Gr/Cu	6.86	7.4	200–300	Sheet
Gr/Al	2.52	6.7	200	Sheet
Dymalloy	5.90	5.5	420	Sheet

^a C10100, C10200 — 1/2H, oxygen free (O₂ < 10 ppm).

The composites CTE are tailorable and are much better matched with Al_2O_3 , AlN , and Si_3N_4 than Cu or Al, thereby greatly reducing thermal stress.

With respect to chemical effects, all the materials being considered should be plated with electroless nickel. Ni plating of 2 to 5 μm ensures good wetting to solders, low moisture absorption rates, and resistance to processing solvents. The cooling liquid should be maintained as neutral, containing 50% glycol. Chemtronics' Flux-Off may be used for cleaning after soldering. These materials are nontoxic.

As for surface finish, it appears they can all be held within the 2 μm range.

Results of preliminary analysis based on CTE only are shown in Table 3.19.

3.2.3.1 Copper/Molybdenum/Copper Laminate

CuMoCu laminate is a popular heat sinking material and is a macrocomposite. Its CTE can be changed from 5.1 to 8.6 by adjusting the ratio of copper to molybdenum in the layered cladding structure. This material is formed in sheets and machined for the specific application.

Table 3.20 shows some property variations with Cu/Mo ratio, from CSM Industries, Cleveland, Ohio.

Although this material has been used for heat transfer in many proven applications, it is rapidly being replaced by the newer, lighter, less-expensive metal matrix composite materials.

Table 3.21 lists Brush Wellman specifications for CuMoCu 13/74/13.

For an apparently similar product, composites vary greatly from one supplier to another for composites that have reached maturity. Therefore, our material specification should include its specific supplier. Amoco supplies both Cu/Mo/Cu and Cu/Invar/Cu composites.

- Weaknesses:
 - High cost
 - High density
 - Difficult to machine
 - Tendency to delaminate

TABLE 3.19

Compatible Substrate Materials

Insulating Substrate	CTE	Compatible Baseplate Material
Alumina (96%)	6.0	Cu/Mo/Cu, Cu/Mo, Cu/W, Gr/Al, Gr/Cu, AlSiC, Dymalloy
Alumina (99%)	7.2	Cu/Mo/Cu, Cu/Mo, Cu/W, Gr/Al, Gr/Cu, AlSiC
Aluminum nitride	4.6	Cu/Mo/Cu, Cu/W, Gr/Al, AlSiC, Dymalloy
Beryllia	7.0	Cu/Mo/Cu, Cu/Mo, Cu/W, AlSiC, Gr/Al, Gr/Cu
Silicon nitride	3.0	Can be used without metal base plate

TABLE 3.20

General Properties vs. Cu/Mo/Cu Ratio

Clad Ratio Cu/Mo/Cu	CTE (ppm/°C)	Thermal Conductivity (W/mK at 25°C)		Density (g/cm ³)	Modulus of Elasticity (GPa)
		X, Y Axis	Z Axis		
5%–90%–5%	5.1	166	150	10.02	303
13%–74%–13%	5.7	208	165	9.84	269
20%–60%–20%	6.5	242	190	9.66	241
25%–50%–25%	7.3	268	213	9.54	220
33 1/3 %–33 1/3 % –33 1/3 %	8.6	311	249	9.36	186

TABLE 3.21

General Properties vs. Cu/Mo/Cu Ratio

Clad Ratio Cu/Mo/Cu	CTE (ppm/°C)	Thermal Conductivity (W/mK at 25°C)		Density (g/cm ³)	Modulus of Elasticity (GPa)
		X, Y Axis	Z Axis		
13%–74%–13%	5.8	181	—	9.9	269

3.2.3.2 Aluminum/Silicon Carbide Metal Matrix Composite

Aluminum/silicon carbide metal matrix composite is a sheet or net-shape material that appears suitable for use with several insulating substrate materials.^{8,10} The net-shape approach to manufacturing complex baseplate shapes appears to yield the highest performance with potentially a low cost-to-performance ratio. Manufacture of most of the net-shape composite materials is accomplished by a three-step process:

- 1. Preform fabrication** — The porous particulate silicon carbide is shaped to its final form using injection molding. The resultant porous AlC perform has all the geometrical attributes of the final base plate. These attributes include cavities, holes, notches, and surface textures of the final base plate. The insulating substrate may be molded into the preform if processing temperatures allow.
- 2. Infiltration** — The porous preform is inserted into a mold that has the dimensions of the final base plate. With vacuum and pressure, molten refractory aluminum infiltrates the porous preform. Various alloys of aluminum and silicon are used to achieve the desired material properties.
- 3. After infiltration** — The baseplate can be flame sprayed with copper on the topside to enhance wetting to the insulating substrate.

TABLE 3.22

General Properties of AlSiC

Supplier	AlSiC Material %SiC	Density (g/cm ³)	CTE (ppm/°C)	Thermal Conductivity (W/mK)	Tensile Strength (MPa)	Young's Modulus (GPa)
Ametek	68 B	3.04	7.5	220	210	
	68 C	3.03	6.8	226	225	
PCC	30		13.8			
	63	3.01	8.5	175 min	253	220
	68	3.03	7.6	175 min	207	255
	74		6.6	200		
MMCC	55	2.97	11.8	190	350	183
CPS	54	2.96	10.13	181.4		167
	63	3.01	7.96	178.1		192
	68, A356.2	2.99	6.88	180		217.5
	68, A383	3.02	6.2	150		
	Cu (102 OFHC)	8.96	17.8	398		117

Table 3.22 shows the material properties of representative net-shape AlSiC materials from various suppliers.

Typical CTE vs. temperature curves for metal matrix composite show that AlSiC CTE is less dependent upon temperature than other materials.

- Weaknesses:
 - Difficult to machine
 - Process dependent

3.2.3.3 Copper/Molybdenum Matrix

Copper/molybdenum composites using refractory molybdenum as reinforcement provide good properties to be used as base plates in power stack designs. By adjusting the copper-to-molybdenum ratio, the coefficient of thermal expansion can be tailored to minimize the mismatch between the baseplate and the die stack. CuMo is produced in sheet form. The rolled CuMo composite material is processed by powder metallurgy technology: starting with molybdenum powder, coating it with copper, and rolling it into sheets. The %Mo is controlled by varying the size of the molybdenum particles.

Table 3.23 shows the properties of CuMo composite material with respect to Cu/Mo ratio.

TABLE 3.23

General Properties vs. Cu/Mo Ratio

Supplier	% Mo	Density (G/cm ³)	CTE (ppm/°C)	TC (W/mK)
Ametek	31	9.32	13.1	275
	64	9.71	9.1	210
	75	9.90	7.8	185
	80	9.94	7.2	175
	85	10.01	6.8	165
Brush Wellman	85	9.6	7.2	145
Spectra-Mat	85	10.02	7.0	160
	80	9.96	8.0	170

The tensile strength specified for Ametek 85% Mo is 80 to 90 Ksi. Other suppliers include Sumitomo and Technical Materials. Pacific Aerospace and Electronics has integrated titanium and CuMo composite, with titanium as the primary material and CuMo only at strategic locations for heat dissipation. The resulting combination achieves light weight, low CTE, and high TC.

- Weaknesses:
 - High cost
 - High density
 - Difficult to machine

3.2.3.4 Copper/Tungsten Matrix

Copper/tungsten composites with refractory tungsten as a reinforcement exhibit good properties to be used as bases in power stack designs. Changing the copper-to-tungsten ratio can tailor the coefficient of thermal expansion to minimize the mismatch between the baseplate and the die stack. Although CuW is generally produced in sheet form, Brush Wellman claims to have developed a net-shape process for this composite material. The process is similar to that of CuMo matrix. The rolled CuW composite material is processed by starting with powdered tungsten, coating it with copper, and rolling it into sheets. There are no sintering aides during processing. The %W is controlled by varying the size of the tungsten particles.

Table 3.24 shows the properties of CuW composite material with respect to Cu/W ratio.

Brush Wellman offers this material in 1" × 1" maximum size. Ametek uses a rolled-sheet process. Other suppliers include L.E.W. Techniques of the U.K., Sumitomo, and Technical Materials.

- Weaknesses:
 - High cost
 - High density

TABLE 3.24

Properties of CuW with Respect to Cu/W Ratio

Supplier	%W	Density (G/cm ³)	CTE (ppm/°C)	TC (W/mK)	Tensile Strength	Modulus (GPa)
Brush Wellman	85–200	16.2	7.1	200	73.5 Ksi	274
	85–150	16	7.1	150	74	275
	90–130	16.9	5.6	130	59	306
Ametek	75	14.87	9.06	205		
	80	15.59	8.21	195		
	85	16.37	7.36	185		
	88	16.95	6.78	180		
	90	16.98	6.51	175		
SMI	80	16.18	7.9	209		
	85	16.72	7.3	197		
	90	17.22	6.7	185		

3.2.3.5 Graphite Fiber-Reinforced Al and Cu Alloys

Composite materials with graphite fibers appear to have excellent potential for high-power applications.¹¹ These materials are very light and can have a thermal conductivity in excess of 1100 W/mK with a CTE range of –1 to –2 ppm/°C. Unfortunately, these composites are relatively new, with little long-term reliability data. These materials are produced in sheets and machined into their final shape. Because graphite is one of the components, these materials machine easily.

One interesting characteristic of graphite-reinforced composites is that their properties can be tailored to fit end usages. For instance, a composite with very high basal plane thermal conductivity can be produced to replace heat-exchange pipe.

The development of these materials should be monitored closely for possible future use. Another composite material of interest is Dymalloy.^{11,12} This is a matrix of copper and carbon (in the crystalline form of diamond). At the ratio 9:11 by volume, Dymalloy has a CTE of 5.5 ppm/°C, a TC of 420W/mK, and a density of 5.9 g/cm³.

Representative properties of graphite bases composites from Ixion Inc. are shown in [Table 3.15](#).

Other suppliers actively involved in the development of these materials are Amoco and Advanced Ceramics.

- Weaknesses:
 - Low tensile strength
 - Relative newness
 - Immature processes
 - Limited availability
 - High cost, especially Dymalloy

TABLE 3.25

General Properties of Graphite Composites

Material	Density (g/cm ³)	CTE (ppm/°C)	TC (W/m K)		Young's Modulus (GPa)	Tensile Strength (Psi)	Flexural Strength (Psi)
			X, Y axis	Z axis			
GrCu 30/70	6.86	7.4	300	200	89	9,000	23,000
GrAl 30/70	2.52	6.7	200	190	88.7	11,150	23,250
Dymalloy	5.9	5.5	420		179		

As these and other graphite materials are developed, their use should be studied and reconsidered.

3.2.4 Production Cost

The lowest-cost practical baseplate material is copper (99% purity, C10200), at less than \$1.00 per square inch finished. To use copper as base plate, proper selection of a good stress-absorbing solder is required. This will be discussed in [Section 3.3.2](#), "Bonding Material."

When combined with molybdenum in laminate form to achieve the desired CTE, the cost is about \$2.00 to \$4.00 per square inch.

Copper/molybdenum composite costs about \$3.00 to \$5.00 per square inch.

Copper/tungsten composite is priced the highest, at about \$5.00 to \$8.00 per square inch.

The cost of aluminum/silicon carbide is about \$1.00 to \$2.00 per square inch. If net-shape is used, there are additional tooling charges of \$10,000 to \$30,000.

Aluminum graphite is quoted at \$3.00 to \$4.00 per square inch, with nickel plating.

3.2.5 Compatible Baseplate/Substrate Material Chart

Based on present technologies, the materials shown in Table 3.26 are currently suitable for use. As new thermal management materials are developed, more can be added to the list.

TABLE 3.26

Compatible Baseplate and Insulating Substrate

Insulating Substrate	CTE	Base Plate
Al ₂ O ₃ (96%)	6	Cu/Mo, AlSiC, Cu ^a
Al ₂ O ₃ (99%)	7.2	Cu/Mo, AlSiC, Cu ^a
AlN	4.6	Cu/Mo, AlSiC, Cu ^a
Si ₃ N ₄	3	Not required

^a Cu can be considered as a candidate if a good stress-relief solder is used.

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3.3 Bonding Material

Bonding provides the vital functions of mechanical, thermal, and electrical linkages between the power semiconductor chips, the terminals, the insulating substrates, and the metal base plate. Therefore, bonding must be properly designed to ensure that the power IGBT module is a mechanically reliable and thermally efficient system. There are two techniques:

- Pressure contact
- Bonding material

3.3.1 Pressure Contact

Pressure contact yields excellent thermal fatigue capability under high-cyclic loads. It also allows double-sided cooling. In general, however, the electrical and thermal contacts are relatively inconsistent, and the production costs are high due to the complicated mechanical structure needed to provide the

mounting force. Also, filling up the case with resin causes problems with pressure contact products. IGBTs, with their large but thin dimensions, present an assembly challenge. In this book, only bonding material will be discussed.

3.3.2 Bonding Material

There are three basic categories of bonding material:¹

- **Organic** — Epoxy, polyamide
- **Metallurgical** — Solder
- **Silver-filled glass** — Glass matrix with silver filler

Table 3.27 compares these types.

Epoxy is a good stress absorber because of its low elastic modulus, but its thermal conductivity is too low. Silver-filled glass has good potential, but its processing temperature of 450°C is a little too high for power-chip assembly. At present, it appears that solder represents the best compromise, especially the soft solder type. Silver-filled glass may be used as a future Pb replacement.

Solders are alloys of two or more metals. When these metals are alloyed together, the melting point of the alloy can be considerably less than the melting point of either of the individual starting metals, a phenomenon which makes the soldering process possible. In the soldering process, the solder is placed between two metal surfaces to be soldered. During melting, the molten solder dissolves a portion of these two surfaces and, when the solder cools, a junction or *solder joint* is formed, joining the two metal surfaces. The metallurgical nature of this joint makes it a stronger bond than either the epoxy or the silver-filled glass.

In the IGBT power module, the solder alloys are used to bond together the metal surfaces shown in Chart 3.1.

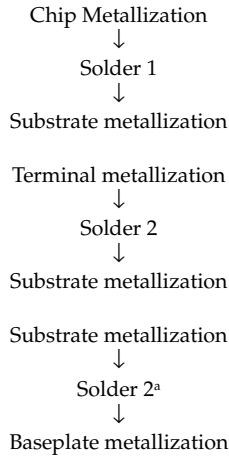
TABLE 3.27

Comparison of Epoxy, Solder, and Silver-Filled (GPa) Glass²

Type	Thermal Conductivity (W/mk)	CTE (ppm/°C)	Elastic Modulus (GPa)	Processing Temperature (°C)	Electrical Resistivity (μΩ-cm)
Epoxy	1–2	50 (< T _g) 200 (> T _g)	3–5	100–150	100
Solder	30–65	20–30		200–350	15
Silver-filled glass	70–80	11	3	400–500	20

CHART 3.1

Soldering of IGBT Power Module



^a The solder can be printed, dispensed, or precoated onto the baseplate metallization.

As will be discussed later, solders 1 and 2 are different alloys. Solder 1 has a higher melting point than solder 2. This is the standard two-solder process. Some manufacturers, however, have used a third solder, lower in melting temperature than solder 2, for the attachment of the terminals to the ceramic. This is done for ease of rework at different stages.

The elements commonly used in solder alloys are:³

- Tin (Sn)
- Lead (Pb)
- Silver (Ag)
- Bismuth (Bi)
- Indium (In)
- Antimony (Sb)
- Gold (Au)
- Copper (Cu)
- Silicon (Si)
- Germanium (Ge)
- Cadmium (Cd)

The most commonly used alloy systems in semiconductor assembly are:

- Au/Sn hard solder
- Sn/Pb soft solder

Other binary alloys include Au/Ge, Au/Si, Pb/In, Pb/Bi, Sn/Ag, Sn/Sb, and Sn/In. Ternary alloys include Sn/Pb/Ag, Sn/Pb/Sb, and Sn/Pb/In. With the continued development of Pb-free solders, more new ternary, quaternary, and pentanary systems have been introduced. So far, the most promising Pb-free solders are Sn/Ag, Sn/Ag/Cu, Sn/Cu, and Sn/Ag/Bi systems. The first two are widely used in U.S. The second and the third are popular in Europe, and the fourth is used in Japan. Matsushita has built its minidisk player using this solder system since 1998.

3.3.3 Selection Criteria for Solder Alloys

Selection of the solder alloys is based on the following criteria:³

- **Melting temperature range in relation to service temperatures** — The selected solder should have a *melting temperature as low as possible* to minimize the thermal stress caused by the TCE mismatch:
 - Upper limit — Due to the CTE mismatch between the power chip, the insulating substrate, and the metal base plate, the processing temperature of the solder should be as low as possible and is preferred to be at or below 350°C. This processing or soldering temperature is typically 20 to 40°C above the solder melting temperature.
 - Lower limit — T_j of the IGBT chip can be as high as 150°C. The solder melting temperature must be at least 10°C higher to prevent any remelting.
 - Processing restrictions — Most power semiconductor modules are assembled using a sequential soldering process. The power chips are first attached to the insulating substrate using a high-temperature solder. The insulating substrate is then attached to the metal baseplate with a lower-temperature solder to avoid remelting of the first solder. This is done so that the two solder attachments can be optimized independently. These two soldering temperatures should be at least 40°C apart. Based on this reasoning, the melting temperature ranges for the two solders should be as follows:
 - First solder — 200 to 310°C
 - Second solder — 160 to 270°C

- **Availability** — The solder should be available in both preform and paste form. The first solder, which is placed between the power chips and the insulating substrate, is often in the form of a *preform*. The preform process is cleaner because there is no chemical involved.⁴ The thickness and coverage are better controlled, so the formation of void is greatly reduced. The preform can be supplied with or without flux and can be Pb or non-Pb based. The second solder, which is positioned between the terminals, the insulating substrate, and the base plate, is usually in the form of *paste*. Here, the surface area involved is much bigger. Substrate warpage, thermal stress, and cost are the primary concerns. Solder paste, which is cheaper than preform, can be deposited as a much thicker layer, which will act as a good stress absorber. Solder paste is usually applied by dispensing or screen-printing. It may also be precoated but at a lower thickness. Most solder pastes have flux available in three versions: no clean, water soluble, and rosin based. The no-clean version is not recommended due to the presence of bare chips. Cleaning steps using solvents to remove the rosin-based flux and its residue must be compatible with the power chips.
- **Eutectic and ternary or lower composition** — Eutectic solder alloys have a single, well-defined melting temperature. Noneutectic alloys, however, have a “plastic” range between the solid and the liquid temperatures. This will result in a less repeatable and controllable process. The “plastic” region should be kept as narrow as possible and preferably < 10°C. Quaternary or higher alloys often have manufacturing control difficulties.
- **Compatibility with the metallization of the power chips, the insulating substrate, and the metal baseplate** — The solder alloys must wet these metal surfaces, which must then be soluble in the solder to form an alloy at the interface. Area of coverage after a DIP test should be > 85%. Excessive leaching of the metallization must be minimized; otherwise, this will create voids. There should also be minimal intermetallic compounds formed, which might have detrimental effects on reliability.
 - Power chip metallization — Ti/Ni/Ag, Cr/Ni/Ag, Al/Ti/Ni/Ag
 - Insulating substrate metallization — Cu + Ni-plating*
 - Baseplate metallization — Cu + Ni-plating, Cu/Mo + Ni-plating, AlSiC + Ni-plating
- **High mechanical strength** — Due to its TCE mismatch with the insulating substrates and the metal base plate, the solder alloy should have:

* Ni-plating provides good solder ability and leach resistance.

- High tensile strength (> 20 MPa)
- High yield strength
- **Low elastic modulus** — This will allow the solder alloy to absorb much of the thermal stress due to the CTE mismatch. The elastic modulus should be < 20 GPa. Silver epoxy has a low modulus, typically about 3 GPa, making it a very good stress absorber. However, its thermal conductivity is only 1 to 2 W/mK, about one-twentieth that of solder.
- **High-creep and high-fatigue resistance** — Permanent deformation as a result of constant stress, either thermal or mechanical, should be as low as possible. Stress required at room temperature to cause failure in 10,000 sec should be > 500 psi. Fatigue resistance, measured in number of cycles to failure, N_f , should be at least 75% of that of Sn/Pb solder.
- **High thermal conductivity** — Because the solder thickness is less than one fifth that of the insulating substrate, the thermal conductivity (k) should be $k \geq 20\text{--}30$ W/mK, to be consistent with that of the insulating substrate, such as AlN.
- **Matching coefficient of thermal expansion (CTE)** — The solder's CTE should be < 29 ppm/ $^{\circ}\text{C}$ to minimize thermal stress caused by mismatch with power chip, substrate, and metal base plate. Most soft-solder systems under consideration have a CTE between 20 and 30 ppm/ $^{\circ}\text{C}$.
- **Electrical resistivity** — The ohmic drop of the solder should be less than 1% of the V_{CESAT} of the IGBT, or ≤ 0.02 V.

$$\rho \leq 10^{-4} \Omega\text{-cm}$$

- **Maturity** — The selected solder alloy should be well understood and acceptable in terms of:
 - Processability
 - Reliability
 - Cost (less than \$10/lb. This means the solder alloy chosen should contain less than 1.5% indium.)
- **Environmental impact** — The solder alloy should exhibit low toxicity and be environmentally friendly, for instance, lead- and cadmium-free. Cadmium is already severely restricted in Europe, and the present industry trend is toward replacing lead. Industry representatives from North America, Europe, and Japan have agreed to eliminate lead solder from manufacturing processes by 2005. In the

European Union (EU), the law banning the usage of lead solders will become effective starting in July 2006.

- **Patent** — Avoid using a patented alloy.

Table 3.28 contains a list of commonly used solder alloys^{3,6–18} in the semiconductor industry. Table 3.29 through Table 3.36 cover the key parameters of the solder alloys for selection.

TABLE 3.28

Common Solder Alloys

Pb Based	Non-Pb Based
43Sn/43Pb/14Bi	42Sn/58Bi
30In/70Pb	71Sn/25Bi/4Ag
60In/40Pb	81Sn/15Bi/4Ag
80Sn/20Pb	30In/70Sn
63Sn/37Pb	60In/40Sn
60Sn/40Pb	96.5Sn/3.5Ag
25Sn/75Pb	95Sn/5Ag
10Sn/90Pb	95Sn/5Sb
5Sn/95Pb	80Au/20Sn
62Sn/36Pb/2Ag	88Au/12Ge
15Sn/82.5Pb/2.5Ag	97Au/3Si
10Sn/88Pb/2Ag	95.5Sn/3.8Ag/0.7Cu
5Sn/93.5Pb/1.5Ag	96.3Sn/3Ag/0.7Cu
5Sn/92.5Pb/2.5Ag	96.2Sn/2.5Ag/0.8Cu/0.5Sb
1Sn/97.5Pb/1.5Ag	99.3Sn/0.7Cu
85Sn/10Pb/5Sb	91.7Sn/3.5Ag/4.8Bi
95Pb/5Sb	93.5Sn/3Sb/2Bi/1.5Cu
95Pb/5In	Sn/Zn/Al ^a

^a Proceed Corporation of Japan introduced this new lead-free solder, with a melting temperature of 190°C, in 2003. It is claimed to be a direct replacement for Sn/Pb solder.

TABLE 3.29

Melting Temperature Ranges of Solder Alloys

Alloy Composition	Liquidus, °C	Solidus, °C	Plastic Range, °C
<i>Pb Based</i>			
43Sn/43Pb/14Bi	163	144	19
30In/70Pb	253	240	13
60In/40Pb	185	174	9
80Sn/20Pb	199	183	16
63Sn/37Pb	183	183	0
60Sn/40Pb	190	183	7
25Sn/75Pb	266	183	83
10Sn/90Pb	302	268	34
5Sn/95Pb	312	308	4
62Sn/36Pb/2Ag	179	179	0
15Sn/82.5Pb/2.5Ag	280	275	5
10Sn/88Pb/2Ag	290	268	22
5Sn/93.5Pb/1.5Ag	301	296	5
5Sn/92.5Pb/2.5Ag	296	287	9
1Sn/97.5Pb/1.5Ag	309	309	0
85Sn/10Pb/5Sb	230	188	42
5Sn/85Pb/10Sb	255	245	10
95Pb/5Sb	240	221	19
95Pb/5In	314	292	22
<i>Non-Pb Based</i>			
42Sn/58Bi	138	138	0
71Sn/25Bi/4Ag	180	180	0
81Sn/15Bi/4Ag	200	200	0
90Sn/3Bi/3.3Ag/3.7In	211	206	5
30In/70Sn	175	117	58
60In/40Sn	122	113	9
96.5Sn/3.5Ag	221	221	0
95Sn/5Ag	240	221	19
95Sn/5Sb	240	235	5
80Au/20Sn	198	198	0
88Au/12Ge	233	233	0
97Au/3Si	304	255	49
95.5Sn/3.8Ag/0.7Cu	218	218	0
96.3Sn/3Ag/0.7Cu	218	217	1
96.2Sn/2.5Ag/0.8Cu/0.5Sb	219	213	6
99.3Sn/0.7Cu	227	227	0
91.7Sn/3.5Ag/4.8Bi	210	205	5
93.5Sn/3Sb/2Bi/1.5Cu	218	218	0

TABLE 3.30

Mechanical Properties of Solder Alloys

Alloy Composition	Ultimate Tensile Strength (10 ³ lb/in ²)	0.2% Yield Strength (10 ³ lb/in ²)	0.01 Yield Strength (10 ³ lb/in ²)	Uniform Elongation (%)	Modulus (GPa)
<i>Pb Based</i>					
43Sn/43Pb/14Bi	5.60	3.60	2.77	2.5	
30In/70Pb	4.83	3.58	3.08	15.1	
60In/40Pb	4.29	92.8	2.06	10.7	
80Sn/20Pb	6.27	4.30	2.85	0.82	
63Sn/37Pb	5.13	2.34	1.91	1.38	18–25
60Sn/40Pb	4.06	2.06	2.19	5.3	18–25
25Sn/75Pb	3.35	2.06	1.94	8.4	
10Sn/90Pb	3.53	2.02	1.98	18.3	19
5Sn/95Pb	3.37	1.93	1.83	26.0	7.4
62Sn/36Pb/2Ag	5.39	2.57			23.2
15Sn/82.5Pb/2.5Ag	3.85	2.40	1.94	12.8	
10Sn/88Pb/2Ag	3.94	2.25	2.02	15.9	
5Sn/93.5Pb/1.5Ag	6.75	3.85	2.40		1.1
5Sn/92.5Pb/2.5Ag	4.03	1.17			9
1Sn/97.5Pb/1.5Ag	5.58	4.34	3.36		1.15
85Sn/10Pb/5Sb	6.45	3.63	2.62		1.40
5Sn/85Pb/10Sb	5.57	3.67	2.26		3.50
95Pb/5Sb	3.72	2.45	1.98		13.7
95Pb/5In	3.66	2.01	1.79		33.0
<i>Non-Pb Based</i>					
42Sn/58Bi	9.71	6.03	3.73	1.3	
71Sn/25Bi/4Ag					
81Sn/15Bi/4Ag					
90Sn/3Bi/3.3Ag/3.7In					
30In/70Sn	4.67	2.54	1.50	2.6	
60In/40Sn	1.10	0.67	0.53	5.5	
96.5Sn/3.5Ag	8.36	7.08	5.39	0.69	5.5
95Sn/5Ag	8.09	5.86	3.95	0.84	
95Sn/5Sb	8.15	5.53	3.47	1.06	
80Au/20Sn	26.56	26.56			59
88Au/12Ge	22.57	22.57			
97Au/3Si	28.84	24.22			83
95.5Sn/3.8Ag/0.7Cu	10.2	7.08			
99.3Sn/0.7Cu					
91.7Sn/3.5Ag/4.8Bi					
93.5Sn/3Sb/2Bi/1.5Cu					

TABLE 3.31

Thermal and Electrical Properties of Solder Alloys

Alloy Composition	Thermal Conductivity (W/mk)	Thermal Expansion (ppm/°C)	Electrical Resistivity ($\times 10^{-6} \Omega\text{-cm}$)
<i>Pb Based</i>			
43Sn/43Pb/14Bi			
30In/70Pb			35
60In/40Pb		26	28
80Sn/20Pb			
63Sn/37Pb	51	24	14.5
60Sn/40Pb	50	24	
25Sn/75Pb			
10Sn/90Pb	36	28	
55Sn/95Pb	32	28	
62Sn/36Pb/2Ag	52	26	15
15Sn/82.5Pb/2.5Ag			
10Sn/88Pb/2Ag	37	29	
55Sn/93.5Pb/1.5Ag			
55Sn/92.5Pb/2.5Ag	39	25	20
15Sn/97.5Pb/1.5Ag			
85Sn/10Pb/5Sb			
55Sn/85Pb/10Sb			
95Pb/5Sb			
95Pb/5In			
<i>Non-Pb Based</i>			
42Sn/58Bi			
71Sn/25Bi/4Ag			
81Sn/15Bi/4Ag			
90Sn/3Bi/3.3Ag/3.7In			
30In/70Sn58			
60In/40Sn			
96.5Sn/3.5Ag	64	30	12.7
95Sn/5Ag	27	23	
95Sn/5Sb			
80Au/20Sn	57	14	17
88Au/12Ge	88	11	30
97Au/3Si	94	12	117
95.5Sn/3.8Ag/0.7Cu			
99.3Sn/0.7Cu			
91.7Sn/3.5Ag/4.8Bi			
93.5Sn/3Sb/2Bi/1.5Cu			

TABLE 3.32

Relative Creep Resistance of Solder Alloys

Alloy Composition	Rank
<i>Pb Based</i>	
43Sn/43Pb/14Bi	Low-moderate
30In/70Pb	Moderate
60In/40Pb	Moderate
80Sn/20Pb	Moderate
63Sn/37Pb	Moderate
60Sn/40Pb	Low
25Sn/75Pb	Low
10Sn/90Pb	Moderate
5Sn/95Pb	Moderate-high
62Sn/36Pb/2Ag	High
15Sn/82.5Pb/2.5Ag	Moderate
10Sn/88Pb/2Ag	Moderate-high
5Sn/93.5Pb/1.5Ag	Moderate
5Sn/92.5Pb/2.5Ag	Moderate
1Sn/97.5Pb/1.5Ag	Moderate
85Sn/10Pb/5Sb	Moderate
5Sn/85Pb/10Sb	High
<i>Non-Pb Based</i>	
42Sn/58Bi	Moderate
30In/70Sn	Low
60In/40Sn	Low
96.5Sn/3.5Ag	High
95Sn/5Ag	High
95Sn/5Sb	High
80Au/20Sn	High
88Au/12Ge	High
97Au/3Si	High
95.5Sn/3.8Ag/0.7Cu	High
99.3Sn/0.7Cu	Moderate
93.5Sn/3Sb/2Bi/1.5Cu	High
93Sn/6In/0.5Cu/0.5Ag	High

TABLE 3.33

Fatigue Resistance of Solder Alloys

Alloy Composition	Melting Temperature (°C)	N _f (cycles)
<i>Pb Based</i>		
63Sn/37Pb	183	3,650
62Sn/36Pb/2Bi	180–183	5,623
63Sn/36Pb/2Bi	177–182	6,982
<i>Non-Pb Based</i>		
96.5Sn/3.5Ag	221	4,186
99.3Sn/0.7Cu	227	1,125
85.2Sn/4.1Ag/2.2Bi/0.5Cu/8In	193–199	10,000–12,000
88.5Sn/3.0Ag/0.5Cu/8In	195–201	> 19,000
93.5Sn/3.1Ag/3.1Bi/0.5Cu	209–212	6,000–9,000
91.5Sn/3.5Ag/1.0Bi/4In	208–213	10,000–12,000
95.4Sn/3.1Ag/1.5Cu	216–217	6,000–9,000
96.25Sn/2.5Ag/0.8Cu/0.5Sb	216–219	6,000–9,000
92.8Sn/0.7Cu/6In/0.5Ga	210–215	10,800

TABLE 3.34Compatibility between Metallizations and Solder Alloys²¹

Metallization		Compatible Solder Alloys
Thick film	PdAg	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag
	PtPdAg	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag
	Au	Pb/In, Au/Sn
Plated copper	Unplated	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag, Sn/Ag/Cu Sn/Ag/Bi, Sn/Cu
	Ni-plated	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag, Sn/Ag/Cu Sn/Ag/Bi, Sn/Cu
Direct bonded copper	Unplated	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag, Sn/Ag/Cu
Active brazed copper		Sn/Ag/Bi, Sn/Cu
Regular brazed copper	Ni-plated	Pb/Sn, Pb/Sn/Ag, Pb/In, Sn/Ag, Sn/Ag/Cu Sn/Ag/Bi, Sn/Cu
Laminated copper	Ni-plated	Pb/Sn, Pb/Sn/Ag

TABLE 3.35Cost¹³ and Maturity of Solder Alloys

Alloy Composition	Metal Cost/in ³	Maturity
<i>Pb Based</i>		
43Sn/43Pb/14Bi	0.75	Good
30In/70Pb		Good
60In/40Pb		Good
80Sn/20Pb		Good
63Sn/37Pb		Good
60Sn/40Pb		Good
25Sn/75Pb		Good
10Sn/90Pb		Good
5Sn/95Pb	1.39	Good
62Sn/36Pb/2Ag		Good
15Sn/82.5Pb/2.5Ag		Good
10Sn/88Pb/2Ag		Good
5Sn/93.5Pb/1.5Ag		Good
5Sn/92.5Pb/2.5Ag		Good
1Sn/97.5Pb/1.5Ag		Good
85Sn/10Pb/5Sb	1.46	Good
5Sn/85Pb/10Sb		Good
95Pb/5Sb		Good
95Pb/5In		Good
<i>Non-Pb Based</i>		
42Sn/58Bi	1.08	Good
30In/70Sn	8.02 ^a	Good
60In/40Sn	2.33	Good
96.5Sn/3.5Ag		Good
95Sn/5Ag		Good
95Sn/5Sb		Good
80Au/20Sn	0.88	Good
88Au/12Ge		Good
97Au/3Si		Good
96.3Sn/3Ag/0.7Cu		New
95.5Sn/3.8Ag/0.7Cu	2.56	New
96.2Sn/2.5Ag/0.8Cu/0.5Sb	1.46	New
71Sn/25Bi/4Ag	2.70	New
81Sn/15Bi/4Ag		New
90Sn/3Bi/3.3Ag/3.7In		New
99.3Sn/0.7Cu		New
93Sn/6In/0.5Cu/0.5Ag	0.92	New
(LF-1 alloy)		New

^a Indium (In) is a precious metal and is very expensive at \$125/lb, vs. \$0.45/lb for Pb and \$3.50/lb for Sn.

TABLE 3.36Non-Pb Based (or Pb-Free) Compositions with Patents²²

Sn	Ag	Cu	Bi	Sb	Zn	In	Other
88–99.35	0.05–3	0.5–6	0.1–3				
90–93.5	2–5	0.3–2	0.5–7				
Balance	1–3	0.5–2	1–10				
Balance	0.1–20		0.1–25			0.1–20	Cu 0.1–3 or Zn 0.1–15
92–99	0.05–3	0.7–6					
Balance	3.5–7.7	1.0–4	0–10		0–1.0		
Balance	0.5–3.5	0.5–2					
Balance	3–5	0.5–3		0.5			

3.3.4 Some Useful Information on Non-Pb–Based (or Pb-Free) Solders

- There is no direct Pb-free replacement for Sn/Pb solder. Any replacement requires changes, from reflow profile and flux management to inspection criteria.
- Six Pb-free systems have been established:
 - Sn/Ag/Bi
 - Sn/Ag/Cu (including Sn/Cu)
 - Sn/Ag/Cu/Bi
 - Sn/Ag/Bi/In
 - Sn/Ag/Cu/In
 - Sn/Cu/In/Ga
- The higher the Sn content, the higher is the opportunity to form tin whiskers and tin oxide, resulting in dross problems. With higher Sn content, the tendency to react with other metals also increases.
- In general, Bi exhibits poor wetting characteristics:
 - > 7% Bi content results in very brittle alloy.
 - Bi is also a poor conductor, both thermally and electrically.
- In and Bi are scarce in supply. Total world availability is 200 tons for In and 4000 tons for Bi, as compared with 240,000 tons for Sn and 10 million tons for Cu. Bi is also a by-product of Pb mining, which will reduce if Pb-based solder is banned.
- High Ag and In content increase cost:
 - Bi ~ \$3.40/lb
 - Sn ~ \$3.50/lb
 - Ag ~ \$85/lb
 - In ~ \$125/lb.

- Ga alloys are expensive and brittle.
- Zn alloys oxidize rapidly and require very strong flux. This may be incompatible with bare power-chip assembly. Zn alloy also has some manufacturing control difficulties.
- When compared with Sn/Pb solder, most Pb-free solders exhibit poorer wetting and slower wetting speed. A stronger flux is used. Flux management must be used to accommodate this.
- The reflow profile needs to be adjusted with a longer liquid time to promote wetting and wider pad coverage for Pb-free solders. Inspection criteria for Pb-free solders are different. Pb-free solder joints are duller and more grainy than those of Sn/Pb. The wetting angle on copper is 36° for Sn/Ag and 43° for Sn/Bi, compared with 17° for Sn/Pb.
- N₂ cover gas is highly desirable for Pb-free alloys to reduce Sn oxidation and to improve wetting.

From the preceding tables and by comparison using the selection criteria, the choices for the first and second solder alloys are shown in [Table 3.37](#).

These choices are by no means the only choices, but they do represent good compromises with the listed selection criteria.

What we have been describing are the *material characteristics of the solder alloys*. Also important are the other components of the solder paste and the manufacturing suitability, processing, and facility conditions.³

3.3.5 Other Components of the Solder Paste

Solder paste can be considered as composed of three components:

- **Solder alloy powder** — Determines the material characteristics of the solder alloy
- **Vehicle system** — Functions as a carrier for the alloy powder, a compatible matrix with the flux system, and a basis for a reliable rheology
- **Flux** — Cleans the alloy powder and the substrates to be joined so that high-reliability metallic continuity results and good wetting can be formed

Both vehicle and flux are nonfunctional after completion of soldering. They are nevertheless crucial to the formation of reliable permanent bonds. On a permanent basis, the solder alloy powder is the only functional component in forming a metallurgical bond. However, the formulation of the solder paste with these three components is important.

Paste applicability depends on its *rheology*, that is, its flow and deformation behavior. This depends on many factors, such as powder size (55, 75, or

TABLE 3.37

Selected First and Second Solder Alloys

	Type	Strength	Weakness
<i>Pb Based</i>			
First Solder	5Sn/95Pb	Mature technology Good stress absorber Good creep resistance Low cost	High M.P. 308–312°C
	5Sn/92.5Pb/2.5Ag	Mature technology Good stress absorber	High M.P. 287–296°C Moderate cost
	5Sn/85Pb/10Sb	Mature technology M.P. 245–255°C High creep resistance Low cost	Plastic region 10°C
Second Solder	63Sn/37Pb	Mature technology M.P. 183°C eutectic Good thermal conductivity Low cost	Average stress absorber
	62Sn/36Pb/2Ag	Mature technology M.P. 179°C eutectic Good creep resistance High tensile strength Good thermal conductivity Presence of Ag reduces intermetallics at interface	Average stress absorber Moderate cost
<i>Non-Pb Based</i>			
First Solder	96.5Sn/3.5Ag	Mature technology M.P. 221°C eutectic Very good thermal conductivity High creep resistance Good fatigue resistance High tensile strength Very good stress absorber With this solder, pure Cu may be used as the baseplate instead of the expansive AlSiC or Cu/Mo Presence of Ag reduces intermetallics at interface	High cost ^a
	95.5Sn/3.8Ag/ 0.7Cu (or 96.3Sn/ 3Ag/0.7Cu) ^b	M.P. 218°C eutectic High creep resistance Good fatigue resistance High tensile strength	High cost ^a New alloy

(continued)

TABLE 3.37 (continued)

Selected First and Second Solder Alloys

	Type	Strength	Weakness
		Very good stress absorber Pure Cu baseplate may be used with this solder. Very good thermal conductivity Presence of Ag and Cu reduces intermetallics at interface	
	95Sn/5Ag	Mature technology M.P. 240°C High creep resistance High tensile strength Very good stress absorber Low intermetallics at interface	High cost ^a Plastic region 19°C Average thermal conductivity
	99.3Sn/0.7Cu	M.P. 227°C eutectic Good creep resistance Low cost	New alloy Poor fatigue resistance May have wetting problem
	93.5Sn/3Sb/2Bi/1.5Cu	M.P. 218°C eutectic Good thermal fatigue High strength	New alloy and quaternary Contain Bi May have wetting problem
Second Solder	93Sn/6In/0.5Cu/0.5Ag	M.P. 180°C	New alloy and quaternary High cost
	81Sn/15Bi/4Ag	M.P. 190°C	New alloy Bi is a by-product of Pb and is in limited supply May have wetting problem Very brittle

^a In general, solder cost is only a small fraction of the total module cost, about 1%.

^b In May 2002, the SPVC lead-free subcommittee recommended 96.5Sn/3Ag/0.5Cu as the alloy to replace the 63Sn/37Pb.

150 μm) and shape, powder concentration, viscosity of the vehicle system, etc. For instance, smaller powder size is preferred for fine-line deposition, a high solder-powder content is beneficial to solder joints but is prone to drying, and a highly viscous vehicle system may improve flow control against temperature yet makes the paste difficult to print or dispense. Paste is also classified into *printable* and *dispensable*. The difference is in the powder concentration or metal content (%), with the lower content ($\sim 85\%$) or less-viscous version more suitable for dispensation.

Commonly used fluxes can be broadly classified into four categories:

- No clean
- Water soluble
- Rosin based
- Synthetic activated

Here, water-soluble flux is the preferred choice. However, sometimes surfaces to be soldered have stubborn barrier layers, such as oxides, hydroxides, sulfides, etc., which tend to impede the wetting and the spreading of the solder. In these cases, rosin-based flux can be used. Rosin-based fluxes are available as follows:

- R (rosin nonactivated)
- RMA (rosin mildly activated)
- RA (rosin activated)
- RSA (rosin superactivated)

Flux percentage in the solder can range from 6 to 25%. Adding very reactive flux may improve solderability, yet it may leave a more corrosive residue and attack the bare power chips. RMA is most commonly used, although the ideal situation is not to use any flux.

3.3.6 Manufacturing Suitability, Processing, and Facility Conditions

- **Compatibility** — With existing production equipment
- **Manufacturing friendliness** — Solder paste stencil life > 4 h
- **Reflow oven profile** — Pb and Pb-free solders have different profiles
- **Processing** — N_2 gas is desirable, especially for Pb-free soldering
- **Storage** — Shelf life > 3 months at 0 to 10°C
- **Working environment** — 18 to 22°C; 40 to 60% RH controlled environment, etc.

Equally important is the quality of the solder suppliers. The solder must be manufactured to meet or exceed the requirements of the Joint Industry Standards. These are the applicable standards:

- IPC - J-STD - 004
- IPC - J-STD - 005
- IPC - J-STD - 006
- IPC-SF-818

- BELLCORE TA-NWT-000078
- ISO 9453
- ISO 9454-1
- ISO 9455-1
- QQ - S - 571

The following is a list of reputable suppliers:

- Solder paste:
 - Advanced Metal Technology (AMTECH)
 - Alpha Metal
 - ESP Solder Plus
 - Heraeus
 - Kester Solder
 - Multicore Solder
- Solder Preform:
 - AIM
 - Coining Corporation of America
 - Gardiner Solder
 - Kester Solder
 - Semi-Alloy
- Epoxy:
 - Ablestik
 - Epoxy Technology
 - AI Technology
- Silver-filled glass:
 - Quantum Materials
 - Amicon

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3.4 Power Interconnection and Terminal Power Interconnection

The most common power interconnection method is wire bonding, using either gold or aluminum wires. In the case of power IGBT modules, heavy aluminum wires are attached between the top aluminum metallization of the IGBT/FRED surface and the Ni metallization of the ceramic substrate by ultrasonic wedge bonding.

Aluminum wires are preferred for power devices for three reasons:

- Larger wire is required to carry high currents associated with power devices. The use of gold wire requires multiple bonds to provide the same current capability as the aluminum wire. Aluminum wire has a very low electrical resistivity of $2.65 \times 10^{-10} \Omega\text{-cm}$.

- Aluminum wire is much cheaper than gold wire.
- The high junction temperature of power chips accelerates the formation of intermetallic compounds. Aluminum wire bonding to the power chips aluminum metallization has no Kirkendall voids and is therefore more reliable than gold wire bonding to the same surface. Aluminum wire bonding to Ni metallization is also highly reliable for high-power and -temperature applications.

Military Standard MIL-M-38510 establishes criteria for maximum current capability for different configurations, as shown in Table 3.38.

Frequently, the maximum current levels from Table 3.38 are further derated by a factor of 0.5 to provide an additional safety factor. For instance, the 0.012" and the 0.022" wires are derated to 10 A and 25 A, respectively, for $L > 0.040$ ".

Instead of pure Al, Al alloys (Al/1%Mg, Al/1%Si) are used as wire material. Al/1%Mg is superior to Al/1%Si in terms of:

- Resistance to fatigue
- Resistance to high temperature

3.4.1 Terminals

There are two approaches used to form the terminals:

- Terminals are formed by soldering to ceramic metallization or by integrating with the case.
- Terminals are formed by extending and bending the ceramic metallization.

TABLE 3.38

Maximum Current History for Aluminum Wire Size

Material	Diameter	Maximum Current (A)	
		$L < 0.040$ "	$L > 0.040$ "
Aluminum (Al/1%Mg)	0.001	0.696	0.481
	0.002	1.968	1.360
	0.005	7.778	5.374
	0.008	15.742	10.876
	0.012	28.920	19.981
	0.015	40.417	27.924
	0.022	71.789	49.600

3.4.1.1 Terminals Formed by Soldering to the Ceramic Metallization or by Integrating with the Case

The properties required of metals used in fabricating the power terminals and fast-on tabs are:^{1,2}

- Low electrical resistivity
- High mechanical strength
- High modulus of elasticity
- High creep resistance
- High wear resistance
- High oxidation resistance
- High corrosion resistance
- Low cost

The following sections summarize the properties of some common metal alloys used for terminals. These are either copper-based or nickel-based alloy.

3.4.1.1.1 Copper Based

Copper-based alloys have the highest electrical conductivity among all alloys. Beryllium/copper (BeCu,¹⁻³ C170, C172), is a commonly used material for terminals due to its good mechanical properties and corrosion resistance. Age-hardened beryllium/copper exhibits high tensile strength of 1500 MPa, hardness, fatigue endurance, and wear resistance. Beryllium/copper can be formed with ease into complex shapes and sharper bends without causing fractures. Corrosion resistance, high electrical conductivity, the highest hardness among copper-based alloys, good wear resistance, and ease of fabrication all contribute to making BeCu a superior material for terminals. The drawback is high cost.

Phosphor/bronze, made with 5% tin and about 0.2% phosphorous, is highly resistant to fatigue and corrosion. It has high tensile strength, can absorb energy, and is wear resistant. Phosphor/bronze has good thermal and electrical conductivity (though only 70% of that of beryllium/copper), and it costs less.

3.4.1.1.2 Nickel Based

Nickel based alloys (Ni 200 and 270) are generally stronger, tougher, and harder than copper-based alloys. Advantages include formability before age hardening, improved stress-corrosion resistance, galvanic compatibility, resilience, low stress relaxation, and the ability to clad or plate.

The most important property is the alloys' ability to retain strength and toughness at high operating temperatures. This property, together with their high module of electricity and fatigue strength, make Ni-containing alloys the preferred material for terminals at high temperature.

Beryllium/nickel contains 1.95% beryllium and 0.5% titanium. Using precipitation hardening, it is the highest-strength nickel alloy from room temperature to 500°C. It has all the properties tested earlier for Ni-based alloys, namely, low stress relaxation at higher operating temperatures, high modulus of elasticity, high fatigue strength, and excellent stress-corrosion resistance. Its electrical conductivity, however, is only one fifth that of beryllium/copper.

Other metal alloys, such as those that are aluminum, cobalt or zinc based, are not as suitable to be terminal material as are copper- or nickel-based alloys. Pure copper has excellent electrical conductivity, corrosion resistance, and low cost, but its tensile strength is only 10% of BeCu.

Tables 3.39, 3.40, and 3.41 summarize the properties and plating characteristics of these metal alloys.

It appears that beryllium/copper and Ni 200 and 270 with nickel plating are all suitable for power module application. Pure copper may be used for power terminals but not for fast-on tabs, which must withstand repeated insertions and withdrawals. The terminals and fast-on tabs can be formed by etching or stamping from a metal alloy sheet.

The power terminals are usually solder attached to the ceramic metallization, either by means of a graphite fixture or by semiautomatic vertical assembly technique. The fixture attachment is performed in a reflow oven, and the solder can either be dispensed or in the form of preform. In the case of Powerex and some Econo-Pak series, the terminals are molded into the case and are connected to the circuitry by wire bonding.

The fast-on tabs are attached to one end of a precut, insulated stranded wire (gauge 14 to 20), with the other end soldered manually to the ceramic metallization.

3.4.1.2 Terminals Formed by Extending and Bending the Ceramic Metallization

The direct-bonded or active-brazed copper metallization on the ceramic substrate can be extended beyond the substrate edge and then bent to form the terminals. The bend can have a pullback from the edges to provide increased isolation needs and a hook shape for stress relief. The Cu metallization is OFHC half hard with a minimum thickness of 12 mils. There is, however, an extension limitation of about 30 mm beyond the substrate edge. This type of terminal is therefore more suitable for low-profile packages, such as the 12-mm high Econo-Pak power module.

TABLE 3.39Copper-Based Metal Alloys²

Property	Alloy 260 Brass	Alloy 172 Beryllium/ Copper	Alloy 510 Grade A Phosphor /Bronze	Alloy 638	Alloy 725	Alloy 762 Nickel/ Silver
Nominal composition	Cu 70 Zn 30	Cu 98.1 Be 1.9	Cu 94.81 Sn 5.0	Cu 95 Al 2.8 Si 1.8 Co 0.4	Cu 88.2 Ni 9.5 Sn 2.3	Cu 59.25 Zn 28.75 Ni 12
Electrical conductivity at 20°C (μmho/cm)	0.163	0.128	0.087	0.058	0.064	
Thermal conductivity at 20°C, (W/m°C)	121	109–130	68.6	40.6	54.4	41.8
Density at 20°C, (g/cm ³)	8.54	8.26	8.86	8.29	8.89	8.70
Modulus of elasticity (GPa)	112	130	112	117	135	127
Yield strength, 0.2% offset, MPa						
Annealed	70–220	109	150	410–470	180	200
Half hard	290–410	123	330–480	530–630	400–510	410–580
Hard	460–530	127	520–620	640–720	520–560	580–680
Spring	580–630	N/A	650–760	700–790	550–650	710–770
Extra spring	600–690	N/A	690–770	750 min	630–720	720 min

TABLE 3.40Nickel-Based Metal Alloys²

Property	Nickel 200	Nickel 270	Duranickel	Be/Ni
Nominal composition	99 Ni	99.97 Ni	93 Ni, 4.5Al	98 Ni
Electrical conductivity μ(mho/cm)	0.106	0.134	0.024	0.027
Modulus of elasticity (GPa)	206	206	206	186–207
Tensile strength (MPa)	379–758	344–655	620–1448	655–1861
Yield strength (MPa)	103–689	103–620	209–1206	275–1586

TABLE 3.41Plating Characteristics for Terminals²

Plating Material	Plating Characteristics
Silver	Silver electrolytes are the most widely used plating for power terminals Will tarnish when exposed to atmosphere, forming silver oxides, and contact resistance will increase
Gold	Excellent corrosion resistance Excellent conductor Low contact resistance Resistance against high-temperature oxidation Solderable High cost
Nickel (electroless)	Good corrosion resistance; fair conductivity Will tarnish; turns yellow after prolonged exposure to a mildly corrosive atmosphere, or turns a green color on severe exposure Generally used as a barrier layer to prevent migration of silver through gold Good wear resistance Contains fewer pores than electrodeposited nickel Low cost
Rhodium	Possesses exceptional wearing resistance Lower electrical conductivity than gold or silver Very expensive Tends to develop microcracks
Tin	Electrodeposits of tin have excellent solderability Good corrosive resistance and is nontoxic Lower electrical conductivity than gold or silver Low cost
Gold over nickel	Good for repeated insertions and excellent corrosion resistance Typical specifications are 25 μ inches of gold over 150 μ inches of nickel
Rhodium over nickel	Excellent wear resistance; high-temperature operation Has higher contact resistance than other platings

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3.5 Encapsulant

Moisture-induced corrosion has an activation energy of about 1 eV for silicon chips. This means that for every 9°C, the rate of the reaction will double. This will greatly affect service lifetime. The chips must therefore be protected.

The basic purpose of the encapsulant is to protect the power chip and wire-assembled components from hostile environments, such as moisture, chemicals, gases, etc.^{1,2} The encapsulant also provides added insulation protection between conductors against increased voltage levels. If the coating is formulated to contain alumina trihydrate powdered filler, then improved resistance to carbon tracking results at high-voltage arcing conditions. If practical, the encapsulant should also serve as a heat-spreading medium. In general, the encapsulants available do not favor rework after encapsulation; therefore, a preencapsulation electrical test is recommended. It should be noted that although these encapsulants are effective in keeping contaminants from the chip and wire assembly, they are also effective in trapping residue contaminants on the chip and wire surfaces. Careful cleaning before encapsulation is vital to ensure long-term reliability. Encapsulation should also be performed in a controlled environment.

IPC-HDBK-830 is the industry standard guideline for design, selection, and application of conformal coatings. Even though this is for surface-mount products, many of the discussions are applicable to power module usage.

3.5.1 Criteria for Selection

- High purity — For direct contact with semiconductor chips
- Low moisture absorption
- Low gas permeability
- Good thermal properties — Good thermal conductivity and CTE; usable temperature range (–50 to 150°C)
- High electrical insulation — Dielectric strength > 250 V/mil
- High mechanical strength
- High chemical resistance
- Manufacturing friendliness — Long pot life; ease of application (either by dispensing or by pouring)
- Cost effectiveness
- Nontoxicity, environmental friendliness, and UL approval

Several classes of coatings that can be considered are:^{1–5}

- Silicone gel
- Silicone

- Polyparaxylylene (parylene)
- Silicon nitride
- Acrylic
- Polyurethane
- Epoxy

3.5.2 Selection

As described earlier, a number of important attributes are desirable when selecting a conformal coating. Because it is in direct contact with bare semiconductor chips, the coating must be sufficiently pure and compatible with the chips. When mixed, it should have a long pot life to allow adequate manufacturing application procedures; it should be easy to apply, adhere securely, and be environmentally safe. When cured, it should not shrink excessively and induce damaging mechanical stress on wires and components. The coating should be a long-term, effective barrier to moisture and chemical contaminants; provide adequate electrical insulation resistance; and not crack under its intended thermal environment. It should have high mechanical strength to lend support to the package and the terminals. Reparability, although a very desirable feature, is generally not practical with most encapsulants applied to chip and wire assemblies.

Presently, there is no single coating that can satisfy all the requirements listed. Some suppliers have adopted a multiencapsulant layer structure to make use of each encapsulant's specific strengths. The multilayer structure is stronger, as expected, but can be heavier than the single-layer structure. There is also the possibility that the top coating will apply downward force on the gel because of thermal expansion. A downward pressure could have a negative effect on long-term reliability. The package structure influences the selection of coatings. If a single-layer structure is used, the package can have an empty space between the chip/wire assembly coating and the top of the package. This allows for a greater choice of coatings. If a multilayer structure is used, the package becomes stronger, but the choice of coatings that are in intimate contact with the electrical components is limited to silicone gels.

3.5.3 Descriptions of Encapsulants

3.5.3.1 *Silicone Gel Encapsulant*

Silicone gel, a thermoset plastic, is the most likely material of choice to be in intimate contact with the semiconductor chips, wires, and substrate. Used as an encapsulant, silicone gels offer many outstanding features, including high purity, high- and low-temperature performance, weatherability and chemical resistance, and low toxicity. Silicone gels, because of their softness, have the

added benefit of providing very little stress to delicate components and the ability to absorb stress caused by thermal expansion of surrounding materials. Their excellent thermal endurance makes them highly desirable for modules that contain heat-dissipating components. These one- and two-part gels can be dimethyl-, phenyl-, or fluoro-based compositions. Dimethyl gels are the lowest-cost general-purpose type for electronic use. Phenyl-based silicones are generally used for very low-temperature applications, whereas fluoro-based gels are used in applications requiring fuel and solvent resistance. Phenyl- and fluoro-based silicones are considerably more expensive.

Because the use of a silicone gel does not allow for repair, a pretest is recommended before encapsulation.

Silicone gels may be somewhat difficult to apply, have a limited pot life, and must be deaired before application. To eliminate voids within the gel before cure, air entrapped during a manual mixing cycle must be removed. To accomplish this, the mixture is placed in a vacuum of 28 to 29 in. of vacuum. As full vacuum is applied, the material will froth and expand to about four times its original volume, crest, and eventually recede back to its original level. The deaeration cycle is completed about 2 min. after the frothing action ceases. The whole process may require 3 to 10 min. There are production static mixers available that mix the two-part gels, so there is no need for separate vacuum deaeration. A static mixer costs about \$10,000.

Note: Silicone gel must be applied in a controlled environment.

3.5.3.2 *Silicone Encapsulant*

Silicone can be used as an overcoat for silicone gel. Intimate contact with the hybrid components would cause long-term reliability problems because of silicone's high coefficient of thermal expansion (70 ppm/°C) and relative stiffness (elastic modulus of 2.2 GPa).

As an overcoat for silicone gel, silicones are very acceptable, primarily because of their chemical compatibility with the gel, both being thermoset plastics. They are especially useful for high-temperature applications. These encapsulants provide high humidity and corrosion resistance along with thermal endurance, which makes them desirable for encapsulating high heat dissipating components. The drawback is a lack of mechanical strength.

Because silicone resins are not soluble and do not vaporize with heat, repair is virtually impossible. Thorough testing of the electronics is recommended before encapsulation.

3.5.3.3 *Parylene Coatings*

Parylene coatings may be the best for all-around durability and reliability. Parylenes are unique in several important ways. First, they are applied in a vapor deposition process under a 0.1-torr vacuum. The deposition occurs at room ambient temperature in a solvent-free atmosphere that places no thermal, mechanical, or chemical stress on the components. The vacuum process requires very specialized vacuum-processing equipment.

A second important unique characteristic is that the highly active gaseous monomer molecules within the vacuum chamber are not hindered by mechanical obstructions. A thin uniform coating occurs on all exposed surfaces, including on sharp corners and edges of components, in tiny crevices, and under components. Typical coating thicknesses are 0.5 to 2 mils, with breakdown voltage of 287 kV/mm (7.3 kV/mil). This uniform coating feature produces a coated area that offers better protection against humid and contaminated environments than most other coatings. However, it provides no mechanical support for the package and the terminals.

The requirement for special vacuum deposition equipment is often a major disadvantage. Because parylene coats all exposed surfaces, the masking procedures of parts such as connectors require great care and process development. This coating should be considered for future use.

3.5.3.4 Silicon Nitride Coating

Silicon nitride is commonly used as a passivation on integrated circuits. This protective coating can also be used as a passivation on chip and wire applications. Plasma deposition systems have been developed to allow low-stress silicon nitride coating to be applied over components on a hybrid assembly. The silicon nitride thickness of approximately 0.5 μm offers excellent protection against humid and contaminated environments. The major disadvantage is the need for specialized processing equipment. Like parylene coating, it provides no mechanical support for the package and the terminals.

3.5.3.5 Acrylic Encapsulant

Acrylics are thermoplastic materials. They are excellent coating systems from a production standpoint because they are relatively easy to apply. Application mistakes can be corrected readily, because the cured film can be removed by soaking in a chlorinated solvent such as trichloroethane or methylene chloride. Acrylic films have desirable electrical and physical properties, and they are fungus resistant. Further advantages include long pot life, which permits a wide choice of application procedures; low or no exotherm during cure, which avoids damage to heat-sensitive components; and no shrinkage during cure. The disadvantages of the acrylics are poor solvent resistance, especially to chlorinated solvents; weak mechanical strength; and low continuous operating temperature of 80 to 100°C.

Acrylics are a poor choice of encapsulant for this application.

3.5.3.6 Polyurethane Encapsulant

Polyurethane encapsulants are available as either single- or two-component systems. They offer excellent humidity and chemical resistance and good dielectric properties for extended periods of time. They are very strong mechanically and lend support to the package and terminals. Resistance to

chemicals also makes repair almost impossible. Like silicone, polyurethane is a thermoset plastic.

Polyurethane may be considered as a top coating if a multilayer approach is used. As a top coating, it offers good mechanical protection, but it does not adhere to the silicone gel. As with silicone gel, vacuum deaeration or static mixers are required to eliminate voids due to trapped air bubbles. Cure cycles are long because of the heat generated during curing. The resulting product should not be operated over 125°C continuously.

3.5.3.7 Epoxy Encapsulant

As a thermoset plastic, epoxy coating provides good humidity resistance and high abrasive and chemical resistance. Like polyurethane, epoxy coatings exhibit excellent mechanical strength. They are virtually impossible to remove chemically for rework, because any stripper that will attack the coating will also attack the other components.

When epoxy is applied, a buffer material, such as silicone gel, must be used around fragile chip components to prevent fracturing from shrinkage during the polymerization process. Curing of epoxy systems can be accomplished at elevated temperatures after the initial overnight room-temperature cure. This extra cure cycle allows for the high exotherm during initial cure stages. Epoxy also requires vacuum deaeration. Deair at 29" Hg until foaming stops. Warming the epoxy to about 60°C will make degassing faster and easier. Epoxies generally have a short pot life. Epoxy resins and hardeners can cause skin rashes, dermatitis, and eye irritation. At elevated temperatures, epoxy may generate vapor that is irritating to the respiratory system. The working area must be well ventilated.

Epoxy may be considered as a top coating if a multilayer approach is used. The resulting product can be operated at or above 125°C continuously.

Table 3.43 gives a generalized guide rating the strengths and weaknesses of selected encapsulants. In the table, an A ranking is the best; D is worst.

TABLE 3.42

Summary of Conformal Coatings' Properties

Material	Tensile Strength (MPa)	Elastic Modulus (GPa)	Conductivity (W/mK)	Coefficient of Expansion (ppm/°C)	Resistivity (Ω -cm)	Dielectric Constant at 1 MHz
Silicone gel	—	—	0.16	—	2×10^{15}	2.7 at 60 Hz
Silicone	10.3	2.21	0.15–0.31	70	10^{15} – 10^{17}	2.9–4.0
Parylene	45–76	—	0.08–0.12	35–69	—	—
Acrylic	12.4–13.8	0.69–10.34	0.12–0.25	50–90	7×10^{13}	v
Polyurethane	5.5–55	0.172–34.5	0.07–0.31	100–200	3×10^8	5.9–85
Epoxy	55–82	2.76–3.45	0.17–0.21	45–65	10^{13} – 10^{16}	3.2–3.8

TABLE 3.43

Conformal Coating Guide

	Silicone Gel	Silicone	Parylene	Silicon Nitride	Acrylic	Polyurethane	Epoxy
Ease of application	B	C	D	D	A	B	B
Removal (chemically)	C	D	—	D	A	B	D
Removal (burn through)	—	D	D	—	A	B	C
Abrasion resistance	B	B	B	D	D	A	A
Mechanical strength	D	C	B	B	D	A	A
Temperature resistance	B	A	A	A	D	D	B ^a
Humidity resistance	B	A	A	A	B	A	C
Pot life	C	D	—	—	A	B	D
Cure, room temperature	C	C	—	—	A	B	B
Cure, elevated temperature	C	C	—	—	A	B	B

^a New epoxy systems have maximum continuous operating temperature over 150°C.

3.5.4 Construction Options

Table 3.44 shows the practical options for the encapsulation of the power module. Table 3.45 summarizes the advantages and disadvantages of the four major encapsulants.

Silicone gel operation must be performed in an environmentally controlled area, such as a laminar hood, because the surfaces of the components must be clean and dry. Silicone gel is usually applied by dispensing to a preset height of about 0.100 to 0.150" above the base plate. This will completely encapsulate the ceramic substrates, the power semiconductor chips and all the aluminum wires. Avoid heat-curing the silicone gel because this will introduce air bubbles. Some suppliers preheat the module to about 60 to 80°C, then apply the gel, followed by vacuum deaeration at 60°C and room-temperature cure until *fully cured*. A partially cured gel has poor solvent resistance, cracks, or edge lifting. The top coating is then applied by either dispensing or pouring until the whole empty space between the silicone gel and the cover is filled. In the case of intelligent power modules (IPMs), the entire control section PCB is embedded in the coating. Cure at any one of the recommended cure cycles. For optimum performance, follow the initial cure with a postcure of 1 hour at 100°C. Alternative cure schedules may also

TABLE 3.44

Practice Options for the Encapsulation of the Power Module

Single-Layer Structure		Multilayer Structure	
Intimate Coating	Top Coating	Intimate Coating	Top Coating
Silicone gel	None	Silicone gel	Polyurethane
Parylene	None	Silicone gel	Epoxy
Silicone nitride	None	Silicone gel	Silicone

TABLE 3.45

Advantages and Disadvantages of the Four Major Encapsulants

Type	Advantages	Disadvantages
Silicone	Operational to 200°C Little or no exothermic heat rise during curing Excellent flexibility Good electrical properties Outstanding environmental resistance Low toxicity High purity	Poor strength May require primer for good adhesion Short pot life
Epoxy	Wide range of cure temperature from below room temperature to 400°F Wide range of viscosities Excellent adhesion Minimal or no volatiles during cure Thermal stability to 200°C Excellent resistance to chemicals Low cost Excellent electrical properties Excellent mechanical strength	Brittle at low temperature Difficult to repair Short pot life Poor resistance to extended period of humidity Shrinkage during curing and polymerization Can cause skin rashes, dermatitis, and eye and respiratory irritation
Polyurethane	Excellent abrasion resistance Good adhesion, low shrinkage Good electrical properties High mechanical strength Excellent environmental resistance Excellent mechanical strength Good pot life	Does not adhere well to silicone gel Maximum continuous temperature 125°C Attacked by some solvents
Acrylic	Excellent resistance to moisture Excellent dielectric properties Excellent arc resistance Excellent reworkability Long pot life Low shrinkage	Poor abrasion resistance Poor mechanical strength Poor chemical resistance Maximum continuous temperature 80 to 100°C

be possible. This product may be cured in large castings with no adverse heat or exotherm effects.

Note: Short all gate and emitter terminals during encapsulation.

3.5.5 Suppliers

- **Silicone gel** — General Electric, Dow Corning, Shin-Etsu
- **Silicone** — General Electric, Dow Corning, Shin-Etsu, Emerson & Cuming
- **Parylene** — Union Carbide, Parylene Coating Services
- **Acrylic** — Emerson & Cuming, Miller-Stephenson
- **Polyurethane** — Conap, Master Bond, Emerson & Cumming
- **Epoxy** — Conap, Emerson & Cumming, Ciba-Geigy

3.5.6 Representative Specifications of Suppliers

Table 3.46 through [Table 3.56](#) show typical properties of encapsulants from different suppliers.

TABLE 3.46

Typical Properties of a Dimethyl-Type Silicone Gel Taken from Shin-Etsu Published Literature

Features	KE 1052 A/B General Purpose	KE 1052 A/B Faster Curing	X-832-050 A/B Fastest Cure	X-832 033-1 A/B Softest
<i>Before Cure</i>				
Appearance		Transparent (all)		
Viscosity, cps, 25°C	1000	1000	750	850
Specific gravity, 25°C		0.97 (all)		
Pot life, 25°C	4 h	30 min	5 min	2 h
Mix ratio		1:1		
<i>Physical Properties</i>				
Cure condition	60 min/ 100°C	15 min/100°C	60 min/ 25°C	4 h/ 50°C
Penetration, 0.10 mm	65	65	70	100
<i>Electrical Properties</i>				
Volume resistivity, ohm-cm		2 × 10 ¹⁵ (all)		
Dielectric strength, kV/mm		20 (all)		
Dielectric constant, 60 Hz		2.7 (all)		
Dissipation factor, 60 Hz		2 × 10 ⁻⁴ (all)		
Operating temperature		-55 to 200°C (all)		
Thermal conductivity, cal/cm/sec°C		3.9 × 10 ⁻⁴ (all)		
Cost	~ \$10/lb	~ \$10/lb	~ \$10/lb	~ \$11/lb

TABLE 3.47

Typical Properties of Silicone Gel Taken from Dow Corning Published Literature

Features	527 Dielectric Gel	3-4150 Dielectric Gel	3-4154 Dielectric Gel	3-6636 Dielectric Gel
<i>Before Cure</i>				
Appearance	Transparent	Trans Green	Transparent	Transparent
Viscosity, 25°C	425	475	545	3250
Specific gravity, 25°C			0.97 (all)	
Pot life, 25°C	90 min	7 min	30 min	30 min
Mix ratio			1:1	
<i>Physical Properties</i>				
Cure condition	20 min/ 125°C	NA	10 min/ 100°C	10 min/ 100°C
Penetration, 0.10 mm	45	50	45	55
<i>Electrical Properties</i>				
Volume resistivity, ohm-cm	7×10^{15}	7×10^{15}	1.05×10^{15}	1.1×10^{15}
Dielectric strength, kV/mm	15.1	15.1	17.7	16.3
Dielectric constant, 60 Hz			2.85 (all)	
Dissipation factor, 60 Hz			0.002 (all)	
Operating temperature			-55°C to 200°C (all)	
Thermal conductivity, cal/cm/sec°C			$< 4 \times 10^{-4}$ (all)	
Cost	~ \$8/lb	~ \$10/lb	~ \$10/lb	~ \$12/lb

TABLE 3.48**Typical Properties of Dow Corning 3140 Silicon Coating**

Type	One-part solventless silicone rubber
Physical form	Ready-to-use viscous liquid
Cure	24–72 h at 25°C & 20% relative humidity
Special properties	Noncorrosive; self-leveling
Primary uses	Dielectric coating of electronic equipment
<i>Typical Properties</i>	
Viscosity, poise	350
Coating thickness	15 mils per dip
Skin-over time	25 min
Tack-free time	1.5 h
Cure time, 25 mils	24 h, 25°C
Cure time, 0.125" thick	72 h, 25°C
Full cure, 0.125" thick	7 days, 25°C
Nonvolatile content	97%
<i>As Cured — Physical</i>	
Appearance	Clear
Specific gravity at 25°C	1.05
Durometer hardness	22 points, Shore A
Tensile strength	300 psi
Elongation	350%
Tear strength	20 ppi, Die B
Peel strength	24 ppiw, primed Al
Volume expansion, 25–100°C	8.8×10^4 cc/cc-C
<i>As Cured — Electrical</i>	
Dielectric strength	500 V/mil
Volume resistivity	5×10^{14} ohm-cm
Dielectric constant at 25°C	2.64 at 100 Hz; 2.63 at 100 kHz
Dissipation factor at 25°C	0.0016 at 100 HZ; 0.0004 at 100 kHz

TABLE 3.49

Properties of STYCAST S 5225 A/B Two-Component Silicone — Properties of Material as Mixed

Property	Test Method	Unit	Value
Mix ratio — Amount of part B per 100 parts part A		By weight	100
		By volume	100
Working life (100 g at 25°C)	ERF 13-70	Hours	4
Density	ASTM-D-792	g/cm ³	1.59
Brookfield viscosity	ASTM-D-2393	Pa.s	2.42
	50 rpm	cP	2420

TABLE 3.50

Cure Schedule

Temperature (°C)	Cure Time
25	16 h
100	1 h
150	30 min

TABLE 3.51

Properties of Material after Application

Property	Test Method	Unit	Value
Hardness	ASTM-D-2240	Shore A	53
Glass transition temperature	ASTM-D-3418	°C	−120
Temperature range of use		°C	−60 to +220
Dielectric strength	ASTM-D-149	kV/mm	17.7
		V/mil	450
Dielectric constant at 1 mHz	ASTM-D-150	—	3.0
Dissipation factor at 1 mHz	ASTM-D-150	—	0.01
Volume resistivity at 25°C	ASTM-D-257	Ohm-cm	1.5×10^{13}

TABLE 3.52

Typical Properties of Parylene Coatings Taken from Parylene Coating Services' Published Literature

Features	Parylene N	Parylene C	Parylene D
<i>Physical Properties</i>			
Density, g/cm ³	1.110	1.289	1.418
Tensile strength, MPa	43	55	62
Water absorption, after 6 h	< 0.10%	< 0.10%	< 0.10%
<i>Electrical Properties</i>			
Volume resistivity, ohm-cm	1×10^{17}	6×10^{16}	2×10^{16}
Dielectric strength, kV/mm	15.1	15.1	17.7
Dielectric constant, 60 Hz	2.65	3.15	2.84
Dissipation factor, 60 Hz	0.0002	0.020	0.004
<i>Thermal Properties</i>			
Melting temperature, °C	410	290	380
Thermal conductivity, W/mK	0.120	0.082	—
Cost	The cost of coating the power module is relatively low because the coating is applied in a batch process. The cost to purchase a parylene deposition system is about \$500,000.		

TABLE 3.53

Typical Properties of Heat-Cure Epoxies Taken from Ciba-Geigy Published Literature

	Araldite CW 5702 US	Hardener HY 5703 US
Viscosity cP	495,000	70
Specific gravity	1.87	1.19
Color	Black	Amber
Mix ratios, by weight		100:30
by vol		100:47
Mixed viscosity, cP		4000
Work life at RT		> 6 h
Cure schedule °C	2.5 h at 90 + 2.5 h at 140	
Shore hardness		95D
Elongation % (at break)		1.1
Tensile strength, psi (at break)		8700
T _g , °C		140
Thermal conductivity, cal/cm-sec °C		15.6 E-04
Coefficient of thermal expansion, °C		40 E-06

TABLE 3.54

Properties of Conap CONAPOXY Epoxy FR-1401 Encapsulation Material

Typical Product Characteristics

	Part A	Part B
Viscosity at 25°C	7500 cps	9500 cps
Specific gravity	1.54	1.57
Color	Black	Tan

Typical Cured Properties

Hardness, shore D	82
Tensile strength, psi	3200
Elongation %	8
Flame resistance, 1/8 inch	UL-94 VO

Electrical Properties, 25°C

Dielectric constant at 100 Hz	5.10
at 1 KHz	4.73
at 1 MHz	4.18
Dissipation factor at 100 Hz	0.065
at 1 KHz	0.039
at 1 MHz	0.017
Volume resistivity — ohm-cm	6.2×10^{15}
Surface resistivity — ohm	2.3×10^{15}
Dielectric strength (0.125" thick), V/mil	> 400

Processing Characteristics

Mix ratio by weight, resin/hardener	1:1
Mix ratio by volume, resin/hardener	1:1
Initial mixed viscosity at 25°C	8700 cps
Work life at 25°C, 200 gm mass	30 min
Peak exotherm, 200 gm mass	101°C
Full cure at 25°C	48–72 h
Cost	\$2.00/lb

TABLE 3.55

Properties of Conap CONATHANES Polyurethane Encapsulation Material

Property	EN-2541	EN-2555
Color — Part A	Dark amber	Clear
Part B	Tan or black	Black
Mixed color	Tan or black	Black
Viscosity at 25°C, cps — Part A	200	198
Part B	30,000	10,840
Mixed viscosity at 25°C	6,000	4,000
Specific gravity at 25°C Part A	1.22	1.08
Part B	1.69	1.62
Mixed system	1.65	1.61
Mix ratio, by weight (rosin/hardener)	16/100	24/100
Pot life at 25°C (1-lb mass)	70 min	35–40 min
Cure time at 25°C	5–7 days	5–7 days
at 60°C	1.5 h	24 h
Peak exotherm at 25°C	40°C	43°C
at 60°C	81°C	100°C
Gel time at 25°C (1-lb mass)	90 min	—
at 60°C	15 min	6 h
Hardness, shore D	70	65
Tensile strength, psi	1,600	2,000
Thermal expansion, in/in/°C	15.1×10^{-5}	11.4×10^{-4}
Volume resistivity, ohm-cm, 25°C	1.6×10^{14}	7.7×10^{13}
Cost	\$5.00/lb	\$6.00/lb

TABLE 3.56

Properties of Miller-Stephenson MS-467N Acrylic Conformal Coating

Electrical Properties

Dielectric strength (volts/mil)	2000
Dielectric constant at 10^5 Hz	3.42
Dissipation factor at 10^5 Hz	0.031

Physical Properties

Glass transition temperature	80°C
Tukon hardness, Knoop no.	13
Acid number	5
Tensile strength (23°C at 50% RH)	11 MPa, 1600 psi
Elongation at break (23°C at 50% RH)	0.5%
Operating temperature	–5 to +80°C

References

1. Harper, C.A., *Electronic Packaging Interconnection Handbook*, 2nd edition, McGraw-Hill, New York, 1997.
2. Pecht, M.G., Agarwal, R., McCluskey, P., Dishongh, T., Javadpour, S., and Mahajan, R., *Electronic Packaging Materials and Their Properties*, CRC Press, Boca Raton, FL, 1999.
3. Speedline Technologies, *Parylene Conformal Coatings, Specifications and Properties* 1998.
4. Dow Corning, *Information about Dow Corning Brand Conformal Coatings*, 2000.
5. Robins, M., Globtop encapsulation for today's packages, *Electronic Packaging and Production*, Feb. 2002.

3.6 Plastic Case and Cover

The plastic case and cover of the module serve five main purposes:

- Mechanical protection
- Environmental protection
- High-voltage creepage and striking distance between terminals
- Mechanical support for terminals (power and fast-on tabs)
- Standardization of electrical and mechanical interface

The power circuitry in the module is interconnected by aluminum wires. Even though these wires are all embedded in soft silicone gel, they can still be broken, lifted, or damaged by mishandling. Environmentally, the module with its power IGBT chips, aluminum wires, and copper metallization are sensitive to moisture, contamination, and chemicals. These will all result in corrosion. The case and the cover provide good protection against mishandling. As for environments, the protection is only of the second or third order. The power IGBT chips are usually processed with a layer of protective coating, such as polyimide, on the surface that is practically hermetic. In addition, the chips, the aluminum wires, the ceramic, and its metallization are all embedded in a layer of silicone gel that provides effective environmental protection. The case and cover also provide anchoring for the terminals and can be designed to offer the necessary creepage and striking distance required by UL508, CSA22.2NO14, and VDE0160. In the case of Powerex, the power terminals are actually molded into the case, the "U-Package." This approach will:

- Eliminate the S bends of the power terminals, thereby lowering the internal inductance
- Eliminate the processing step of attaching the power terminals, thereby reducing the assembly cost

For this approach to work, the molding compound is usually mixed in with fillers, such as silica, glass, or Al₂O₃, to match the expansion coefficient with those of the metal terminals.

The case and cover are usually processed with a B-staged epoxy film applied to the open edges. When attaching to the module, this film can be reflowed and cured to yield a highly reliable bond. Typical film thickness is 2 to 5 mils, and a uniform clamping pressure (1 to 10 psi) should be applied during curing. The adhesion surface must be smooth, clean, and dry. The case is typically 50 to 70 mils thick and is usually designed with a lip overhanging the edges of the baseplate to increase the surface area of adhesion. Some suppliers also have cut-offs at the mounting holes to avoid possible fracture caused during bolting down to the heat sink. The cover can also be attached to the case by mechanical snap-on or through tight fit with the terminals.

Two of the industry standards, as illustrated in [Figure 3.1](#) and [Figure 3.2](#), are:

- Int-A-Pak
- Double Int-A-Pak

Based on the preceding usages, the following is a list of selection criteria for the case and cover material:

- High mechanical strength
- Rigid and sturdy enough for continual handling
- Flexible enough to ensure proper mating with other parts of the module
- Dimensionally and thermally stable from -50 to +125°C
- Low mold shrinkage
- Low water absorption
- Resistance to chemicals
- High and stable dielectric strength
- High arc resistance
- High volumetric and surface resistivity
- Flame retardant to UL-94VO standard
- Low outgassing
- No health hazard
- Economical cost

INT-A-PACK

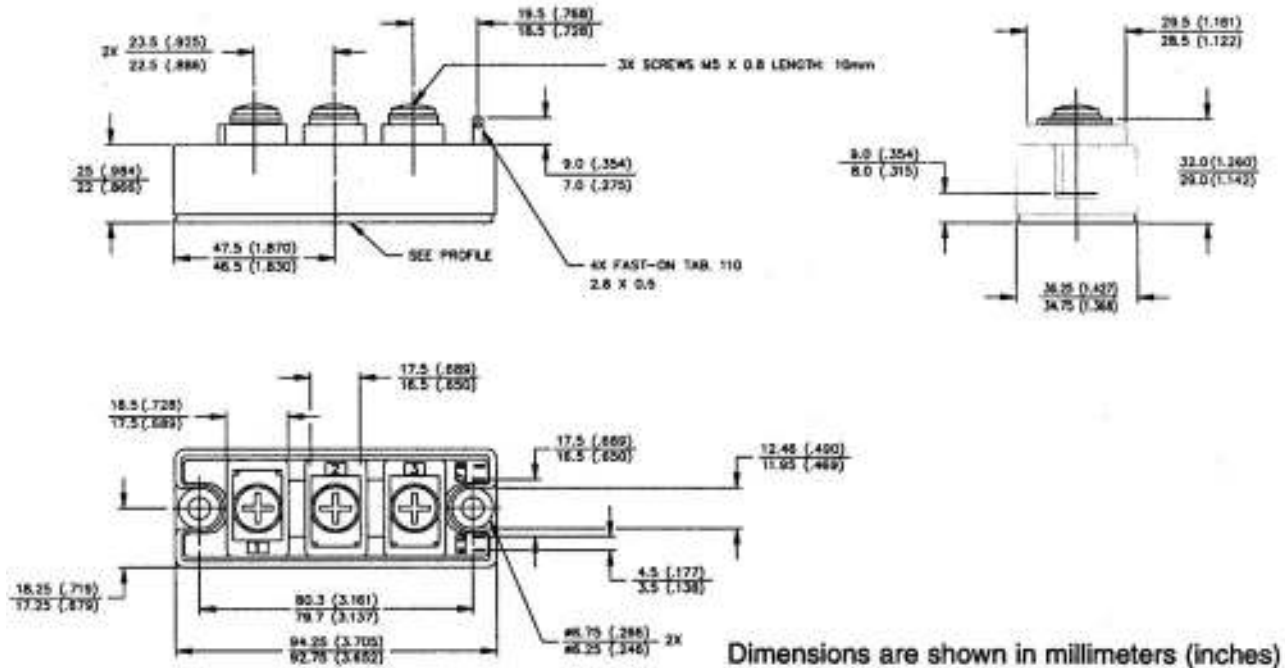


FIGURE 3.1

Int-A-Pak case outline. (Used with permission from the International Rectifier Corporation.)

INT-A-PACK

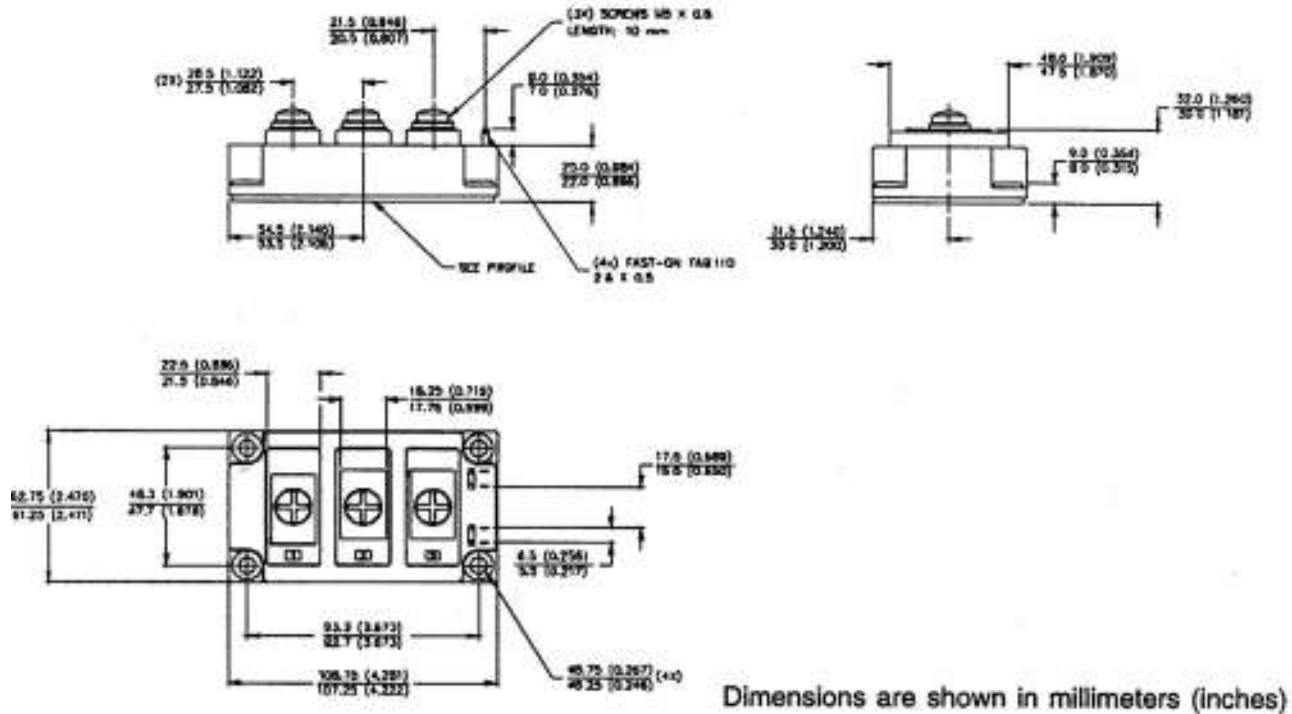


FIGURE 3.2

Double Int-A-Pak case outline. (Used with permission from International Rectifier Corporation.)

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Numerous plastic materials are available for packaging applications.^{1,2} The following is a list of some of the popular ones:

- Thermosets:
 - Alkyd
 - Allyl
 - Epoxy
 - Melamine
 - Phenolic
 - Polyimide
 - Silicone
- Thermoplastics (amorphous and crystalline):
 - ABS
 - Acetals
 - Acrylics
 - Cellulosics
 - Fluoroplastics
 - Liquid crystal polymer
 - Nylon
 - Parylene
 - Polycarbonate
 - Polyester
 - Polyetherimide
 - Polyethersulfone
 - Polypropylenes

Among these choices, the following materials have been used by various suppliers:

- **Thermoset allyls** — Diallyl phthalate (DAP) with glass filler
- **Thermoset epoxy**
- **Thermoplastic polyester** — Polybutylene terephthalates (PBT) with glass filler

Table 3.57 shows the typical properties of these three materials. These properties can be changed or adjusted by adding fillers, such as the following:

- Glass fiber
- Mineral

- Metal
- Fiber
- Organics

However, filler additives represent a compromise in performance. For instance, a glass-filled epoxy will increase its tensile and impact strength but will also increase its viscosity, which is not desirable for producing thin-wall modules.

The following is a list of possible suppliers for materials and service:

- Plastic material:
 - Union Carbide Chemicals and Plastics
 - Dupont
 - Climax Performance Materials
 - Dow Chemical
 - Mobile Chemical
- Case and cover fabricators:
 - Poly-Hi
 - Robinson Electronics
 - Mobile Chemical
- B-staged epoxy:
 - Ablestik — Ablebond 961-2
 - A. I. Technology — 7355, 7675
- Regular epoxy:
 - Cotronics — Bond-it 750
 - Ablestik — Ablebond 961-2
 - A. I. Technology — 7675

TABLE 3.57

Properties of Three Commonly Used Materials for Plastic Case and Cover¹⁻³

	DAP	Epoxy	PBT
Dielectric strength (V/mil)	350	360	420
Volume resistivity (-cm)	10 ¹³	3.8 × 10 ¹⁵	1.4 × 10 ¹⁵
Arc resistance (seconds)	130	140	190
Water absorption (% 24 h)	< 0.2	0.2	0.09
Tensile strength (lb/in ²)	8,500	30,000	8,500
Specific gravity	1.84–1.91	1.8	1.31
Impact strength (ft lb/in)	0.85	10	1.0
Heat deflection temperature (°F)	500	400	130
Health hazard	None	Dermatological problems	None ^a
Cost	Medium	Low	Low

^a Widely used in the medical field due to its stability, toughness, and resistance to chemicals.

References

1. Pecht, M.G., Agarwal, R., McCluskey, P., Dishongh, T., Javadpour, S., and Mahajan, R., *Electronic Packaging Materials and Their Properties*, CRC Press, Boca Raton, FL, 1999.
2. Harper, C.A., *Electronics Packaging and Interconnection Handbook*, 2nd edition, McGraw-Hill, New York, 1997.
3. Robison Electronics, Inc., Tolerances and Materials: Diallyl Phthalate Properties.

3.7 Power Semiconductor Chips

Most power modules currently are manufactured using one or a combination of the following four types of power semiconductor chips.

3.7.1 IGBT Chip

The key parameters for the IGBT chip are:

- **Conduction loss** — Represented by the saturation voltage, V_{CESAT}
- **Switching loss** — E_{off}
- **Short circuit ruggedness** — Represented by tsc, short-circuit endurance time

The performances of these parameters represent a trade-off in the design of the IGBT chip.¹ For instance, the switching loss is reduced as carrier-injection efficiency is increased and the carrier lifetime is decreased. On the other hand, the conduction loss is just the opposite; it increases. Similarly, improvement in short-circuit ruggedness by using thicker and homogeneous starting material will result in an increase of V_{CESAT} . As technology evolves, new techniques emerge that help to reduce V_{CESAT} without adversely affecting the other two. As a result, the trade-off window improves considerably.

The trade-off is basically controlled by three factors:¹⁻⁷ body structure, gate structure, and process control.

3.7.1.1 Body Structure

- Punch-through (PT):
 - Regular multiepitaxial structure
 - Silicon direct bonding (SBD) structure — Direct bonding of two homogeneous wafers

- Soft punch-through (SPT) structure — A compromise between PT and NPT structures; use of homogeneous wafers
- Non-punch-through (NPT-U):
 - Ultrathin homogeneous floating-zone wafer structure
- Non-punch-through (NPT-R):
 - Regular homogeneous floating-zone wafer structure

Figure 3.3 shows different IGBT body structures.

Note: Both SDB and SPT belong to the PT structure. In the case of SPT, the n-drift region thickness is between PT and NPT-U.

Most IGBT manufacturers use 6" wafers to process IGBT chips. The thinning of a 6" wafer to a thickness between 80 and 100 μm for 600 V and between 150 and 175 μm for the 1200 V version with tolerable warpage represents a major challenge. At the 32nd European Microwave Week conference, Agere Systems was reported to have processed an RF power transistor chip as thin as 40 μm . There are basically four available techniques.

3.7.1.1.1 Grinding⁸

Grinding has now replaced lapping for thinning the next-generation silicon wafers. It provides tighter control over mechanical dimensions and lower subsurface damage. Ultraprecision grinders are now available in the market.

IGBT STRUCTURE

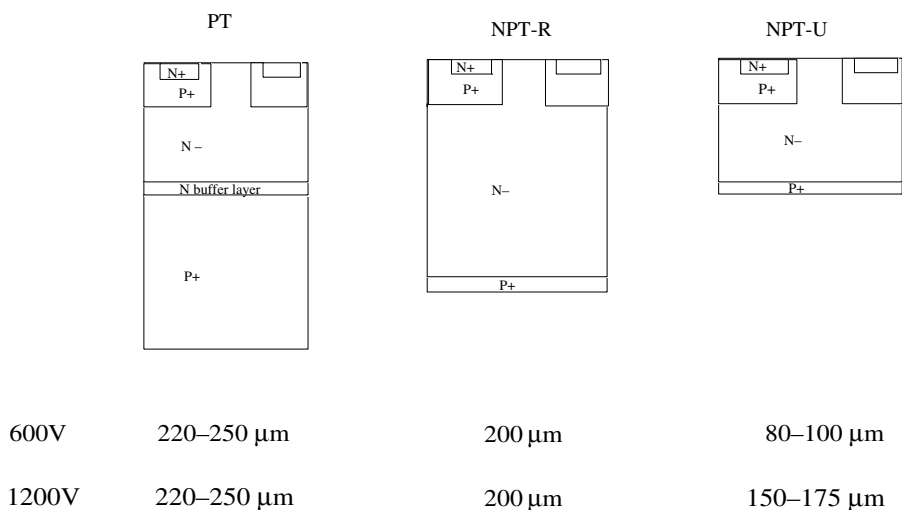


FIGURE 3.3
IGBT structure.

These grinders use silica particles (0.01 to 0.02 μm in diameter) as the grind wheel abrasive. The surface finish is comparable with a polished surface. *In situ* thickness measurement is also used to obtain a closed-loop control of thickness.

3.7.1.1.2 Localized Thinning⁹

Here, only the IGBT areas of the wafer are thinned. The thicker border between chips provides structural support. This technique has been used to produce an ultrathin photovoltaic solar cell.

3.7.1.1.3 Plasma-Assisted Chemical Etch (PACE)¹⁰

Unlike grinding, this is a noncontact material removal technique. It is a dry etch using freon (CF_4) gas with no wet chemical involved. It operates at atmospheric pressure and etches at a rate of about 1 to 2 $\mu\text{m}/\text{min}$.

3.7.1.1.4 Spin-Etch

This is an etching technique developed by SEZ. The wafer is placed on a wafer chuck with the side to be thinned facing up. The chuck is then rotated at very high speed, and a dispensing arm applies the etch mixtures to the wafer. Due to the high rotation speed, the etchant is distributed evenly on the wafer. SEZ claims to have processed a 300-mm wafer to a thickness of 4 mil or 100 μm . SEZ offers the spin-process system for 4- to 12-inch wafers in single- and multiple-chamber designs.

3.7.1.2 Gate Structure^{4,5}

- Conventional MOS gate design:
 - Simple process
 - Regular cell density
- Self-aligned design:
 - Simplest process
 - High cell density results in low V_{CESAT}
- Trench gate design:
 - Complicated process
 - Highest cell density results in very low V_{CESAT}

3.7.1.3 Process Control

- Uniform carrier lifetime control:
 - Low switching loss (entire chip)
 - High V_{CESAT}

- Localized carrier lifetime control:
 - Low switching loss (at the n-buffer layer)
 - Low V_{CESAT}
- No carrier lifetime control:
 - Low V_{CESAT}

The first generation of IGBT devices used a punch-through epitaxial structure with a conventional MOS gate design and uniform carrier lifetime control. This resulted in a 100 A IGBT of 3.5 V for a 1200-V and 2.5 V for a 600-V IGBT. The latest, or fourth, generation has drastically reduced the V_{CESAT} by using one of the following four combinations: ²⁻⁶

- PT + trench gate + localized carrier lifetime control
- PT + self-aligned + localized carrier lifetime control
- NPT-U + trench gate + no carrier lifetime control
- NPT-U + self-aligned + no carrier lifetime control

Table 3.58 compares the V_{CESAT} of the first and fourth generations IGBT. Table 3.59 shows a list of IGBT suppliers and their respective technologies based on recent publications. Because this information is derived from publications, its accuracy may be questionable. This summary is intended only as a reference, because technology and design change rapidly in this field.

Table 3.60 lists some of the IGBT chips offered by five suppliers:

- APT
- IR
- IXYS/ABB
- Siemens
- Dynex

The emitter metallization is aluminum alloy for aluminum wire bonding. The backside metallization is typically Ti/Ni/Ag, Cr/Ni/Ag, or Al/Ti/Ni/Ag for soldering.

Most of the designs have multiple bonding pads, arranged in a matrix formation (2×2 , 2×3 , 2×4 , etc.; see IGBT chip topography). For an emitter pattern with a whole metallization, such as IR, the aluminum wires should

TABLE 3.58

V_{CESAT}

	First Generation	Fourth Generation
600 V	2.5 V	1.6 V
1200 V	3.5 V	1.9–2.5 V

TABLE 3.59

Summary of Suppliers' Technologies

Supplier	Technology
Dynex	PT + trench gate + localized lifetime
APT (Power MOSFET)	NPT-U + self-aligned
Fuji	PT + self-aligned + localized lifetime (≥ 600 V) NPT-R + self-aligned (≥ 1200 V)
Eupec/Infineon (IGBT ³)	NPT-U + trench gate
IR	NPT-U + self-aligned
Hitachi (GR-series)	PT + trench gate + localized lifetime (≥ 600 V) PT + self-aligned + localized lifetime (≥ 1200 V)
Powerex/Mitsubishi (F-series)	Soft PT + self-aligned + localized lifetime
(NF-Series)	Carrier-stored trench gate (CSTBT)
IXYS (NPT ³)	NPT-U + self-aligned
Samsung	SBD
Toshiba (IGBT ⁺⁺)	NPT-R + self-aligned

TABLE 3.60

IGBT Chips

Supplier	Size	Ratings
APT	0.199" $\times$ 0.203"	25–35 A, 600–1000 V
	0.260" $\times$ 0.260"	40–50 A, 600–1000 V
	0.254" $\times$ 0.414"	50–75 A, 600–1000 V
	0.388" $\times$ 0.588"	90–130 A, 600–1000 V
	0.588" $\times$ 0.738"	200–300 A, 600–1000 V
IR	0.091" $\times$ 0.139"	10 A, 600 V
	0.116" $\times$ 0.175"	20 A, 600 V
	0.170" $\times$ 0.228"	30 A, 600 V
	0.257" $\times$ 0.257"	40 A, 600 V
	0.257" $\times$ 0.360"	60 A, 600 V
	0.523" $\times$ 0.523"	100 A, 1200 V
IXYS	0.259" $\times$ 0.259"	30 A, 600 V
	0.284" $\times$ 0.351"	45 A, 1200 V
	0.284" $\times$ 0.375"	35 A, 1400 V
Siemens	0.258" $\times$ 0.258"	25 A, 1200 V
	0.354" $\times$ 0.354"	50 A, 1200 V
	0.438" $\times$ 0.438"	75 A, 1200 V
	0.500" $\times$ 0.500"	100 A, 1200 V
Dynex	0.260" $\times$ 0.260"	25 A, 1200 V
	0.280" $\times$ 0.360"	35 A, 1200 V
	0.534" $\times$ 0.534"	100 A, 1200 V

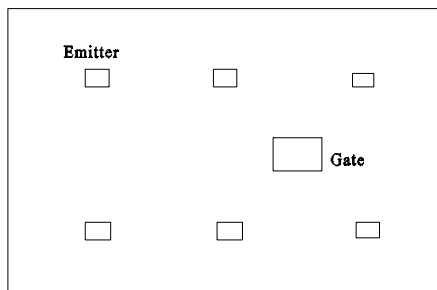
have intermediate stitches across the chip. This is to ensure a more uniform current distribution during operation. Figure 3.4 and Figure 3.5 show APT, IR, and IXYS chip topography.

The selection of the specific IGBT chip depends to a large extent on the application or on the market intended to serve. Currently, the IGBT module

IGBT CHIP TOPOGRAPHY (APT & IR IGBT CHIP)

APT

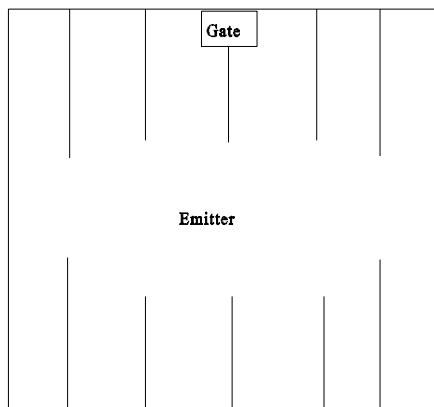
90–130A, 600–1000V



0.388" 0.588"

IR

100A, 1200V



0.523" × 0.523"

FIGURE 3.4

IGBT chip topography (APT and IR IGBT chip).

IGBT CHIP TOPOGRAPHY (IXYS)

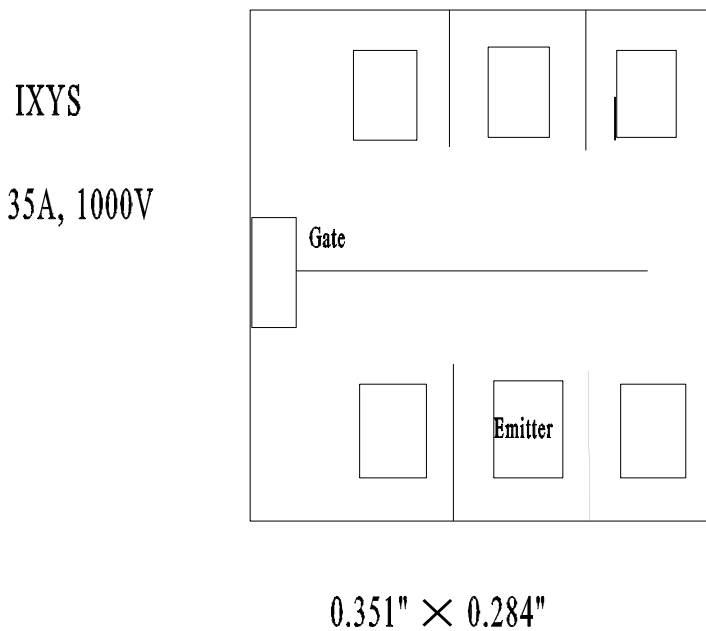


FIGURE 3.5
IGBT chip topography (IXYS IGBT chip).

is used mainly as a switching component in the inverter circuits for both power supply and motor drive applications.

- Power supply:
 - UPS
 - Switching power supply
 - Welder
 - Induction heater
 - Medical equipment
- Motor drive:
 - HVAC
 - Elevator
 - Robotics
 - AC Servo

The power-supply applications emphasize lower switching and conduction losses, whereas motor-drive applications usually demand short-circuit

TABLE 3.61**Punch-Through (PT)**

Epitaxial wafer	Higher material cost
Thick wafer	Ease of handling Lower mechanical breakage
Low V_{CESAT} and negative temperature dependence	
Less rugged	
Heavy ion irradiation for localized lifetime control	Lower switching loss Short tail current Higher leakage current More temperature dependence of leakage and switching characteristics Higher processing cost
Trench gate	High cell density and very low V_{CESAT} Reduction in chip size Limited short-circuit withstanding capability Higher processing cost and lower yield
Soft punch-through (SPT)	Nonepitaxial, float zone wafer, no lifetime control Compromise between PT and NPT-U in terms of V_{CESAT} , switching loss and ruggedness Positive temperature dependence of on-state

ruggedness. For applications that require paralleling of IGBT devices, positive temperature dependence of on-state is preferred to facilitate current sharing.

As discussed earlier, the basic behavior of the IGBT device is controlled by three factors:

- Body structure
- Gate structure
- Process control

Table 3.61 through [Table 3.63](#) show a rough categorization of the IGBT device according to its body structure, combined with different gate designs and process control.

IGBT suppliers have been blending body structure with different gate designs and process controls to optimize the final performance. For instance, Eupec has offered IGBT³, which is a combination of NPT-U and trench-gate technologies; Powerex has introduced a 1700-V IGBT product using SPT technology but with heavy ion lifetime control; and IR's WARP IGBT is a special epitaxial structure with localized lifetime control. Suppliers have also started applying a 1- μ m-or-less design rule to increase cell density, thereby lowering the V_{ON} .

TABLE 3.62**Non-Punch-Through (NPT-U)**

Homogeneous float-zone wafer	Lower material cost
Ultrathin wafer	Difficult to handle Higher mechanical breakage High processing cost
Higher V_{CESAT} and positive temperature dependence	
Rugged	
No lifetime control	High switching loss Long tail current Low leakage current Less temperature dependence of leakage and switching characteristics Tighter parameter distribution

TABLE 3.63**Non-Punch-Through (NPT-R)**

Homogeneous float-zone wafer	Lower material cost
Regular thickness	Ease of handling Lower mechanical breakage
Highest V_{CESAT} and positive temperature dependence	
Very rugged	
No lifetime control	Higher switching loss Very long tail current Lowest leakage current Less temperature dependence of leakage and switching characteristics Tighter parameter distribution

STMicroelectronics' Power Mesh strip-layout process claims to have a cell density of 5 to 7 million cells per square inch and a channel density of 6200 cm per square centimeter. As for the high-voltage passivation, a common technique is to use SIPOS on oxide, combined with field plate, field ring, or variable lateral doping (VLD).

3.7.2 FRED (Fast Recovery Epitaxial Diode) Chip

FRED is an essential element in the circuit. For it to perform its functions properly, the following two characteristics are required to reduce snappy recovery:¹¹

- Fast recovery — Reduces turn-on switching loss t_{rr} to less than 100 ns at 25
- Soft recovery — Minimizes voltage overshoot to eliminate snubber circuit $t_a/t_b \sim 1$

Figure 3.6 shows typical reverse recovery characteristics of a FRED.

FRED technology uses high-voltage epitaxial silicon combined with a shallow P diffusion for low forward voltage drop. Guard ring termination is often used to minimize leakage current, guarantee stable breakdown voltage, and improve reliability of the diode.

Fast recovery and soft recovery are generally achieved by using a special carrier lifetime control process: platinum diffusion as opposed to the more common gold diffusion or electron irradiation. Platinum provides lower leakage current at high temperatures and faster recovery time at high forward current but higher forward voltage drop.

Table 3.63 lists some of the FRED chips offered by APT, IR, IXYS, Siemens, and Dynex.

A typical FRED chip topography is shown in Figure 3.7.

The backside metallization for these chips is typically Ti/Ni/Ag or Al/Ti/Ni/Ag. The top metallization is again aluminum alloy for wire bonding. Appendix A lists power MOSFET, Thyristor, and Rectifier chips for power modules.

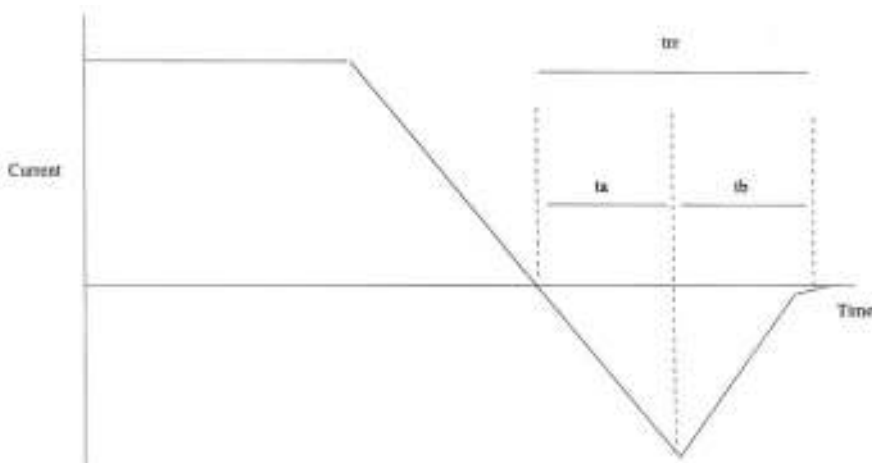


FIGURE 3.6

Typical reverse recovery characteristics of a FRED.

TABLE 3.64

FRED Chips

Supplier	Size	Ratings
APT	0.085" × 0.180"	15 A, 400–1000 V
	0.120" × 0.255"	30 A, 400–1000 V
	0.248" × 0.248"	60 A, 400–1000 V
	0.270" × 0.416"	100 A, 400–1000 V
IR	0.169" × 0.220"	32 A, 1200 V
	0.360" × 0.360"	100 A, 1200 V
IXYS	0.244" × 0.244"	60 A, 1000 V
	0.284" × 0.351"	75 A, 1000 V
Siemens	0.140" × 0.260"	25 A, 1200 V
	0.220" × 0.220"	35 A, 1200 V
	0.256" × 0.256"	50 A, 1200 V
	0.300" × 0.300"	75 A, 1200 V
Dynex	0.380" × 0.380"	100 A, 1200 V
	0.140" × 0.200"	25 A, 1200 V
	0.200" × 0.240"	35 A, 1200 V
	0.508" × 0.508"	200 A, 1200 V

FRED CHIP TOPOGRAPHY

Size 6



(.270" × .416")

(10.57mm × 6.86mm)

100 Amps

400, 600, and 1000 Volts

FIGURE 3.7
FRED chip topography.

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Manufacturing of Power IGBT Modules

The assembly of the basic power IGBT module (or the power section of the intelligent power IGBT module IPM) is made up of cleaning, solder attaching, power interconnecting, dispensing, and encapsulation hybrid circuit processes. The specific nature and details of these processes will be described in this chapter. During production, the processes are closely monitored by inspection sites that are positioned strategically along the entire assembly line. This ensures that the final product meets the initial design goal or specifications. The finished products are stress screened, fully tested, and then sample life tested to guarantee long-term reliability. Also, to achieve as much of a void-free solder attachment as possible and to avoid damaging the sensitive IGBT gate oxide structure, strict requirements are imposed on manufacturing facilities.

The standard manufacturing processes for the 200 A IGBT module are solder attachment by oven reflow and power interconnecting by ultrasonic aluminum wire bonding. For reasons of reliability and cost, an alternative manufacturing process will be presented that uses an all-solder assembly. The flow charts in [Section 4.4](#) compare these two processes.

This chapter is divided into four sections:

- Manufacturing Process
- Process Control/Long-Term Reliability
- Manufacturing Facilities
- Manufacturing Flow Charts

4.1 Manufacturing Process

The manufacturing process for the power section consists of the following major operations:

- Sorting/grouping of the IGBT chips
- Cleaning
- Dispensing or printing of solder paste
- Attaching the power IGBT/FRED chips to the ceramic substrate
- Attaching ceramic substrate to the metal baseplate
- Wire bonding
- Attaching power terminals to the ceramic substrate
- Attaching fast-on tabs to the ceramic substrate
- Attaching plastic housing and lid
- Coating with silicone gel and epoxy
- Electrical and thermal testing
- Barcoding (or 2D data matrix coding)
- Marking (or attaching labels)

Ideally, the whole production should be performed in a class 1000 or better environment. However, constructing and maintaining a large cleanroom of this class level is expensive. The trend is therefore toward having multiple small, isolated units of controlled environment, such as a vinyl wall modular cleanroom, cleanbooth, or laminar hood, in the main processing area where the level is maintained at 100,000.

Inside these controlled units, the following operations can be performed in the environment where class 1000 or better is achievable:

- Cleaning
- Dispensing (or printing) of solder paste
- Attaching components — Power chips, ceramic substrate, power terminals, base plate
- Al wire bonding
- Coating with silicone gel

The parts may be transported between these units in small, clean containers known as *minienvironments*. These containers are made of antistatic, low outgassing material and can be either sealed or purged-gas types. The gas should be ultradry for transporting passive parts, such as ceramic, metal base plate, and terminals, but for chips or subassembly it should be at 40 to 60% RH.

Most IGBT OEMs manufacture the module products in lots, with lot size ranging from 20 to 150 units. Each lot is assigned a lot number. For traceability requirements, a lot should contain all relevant information on the following:

- Components used
- Processes used

- Equipment used
- Facilities conditions
- Inspection data
- Testing data
- Date and operator

This information can be recorded in a lot traveler or in the lot database.

The following sections will concentrate on five operations, which have direct impact on yield and product performance:

4.1.1 Sorting and grouping of the IGBT chips

4.1.2 Cleaning

4.1.3 Solder attachment

4.1.4 Power interconnection

4.1.5 Electrical and thermal testing

There are different processing methods that may be used to do each of these assembly steps. The major deciding factors in the choice of a method are based on consideration of the following factors:

- Manufacturing capacity
- Manufacturing yield
- Manufacturing cost
- Manufacturing cycle time
- Environmental requirements
- Product performance and reliability

4.1.1 Sorting/Grouping of the IGBT Chips

[Chapter 5](#), Design, presents the benefits of constructing the 200 A power IGBT module by paralleling two 100 A chips (2×100 A). However, paralleling a power IGBT is not a trivial matter. Items that must be considered are:

- Current imbalance
- Junction temperature imbalance

4.1.1.1 Current Imbalance

There are no two identical chips. The forward voltage, V_{CEON} ([Figure 4.1](#)), will be different for any given current level. When two IGBT chips are paralleled, the V_{CEON} s across both chips are forced to be the same. Thus, for any given load current, one IGBT will carry more current than the other,

IGBT in V_{CEON} MODE

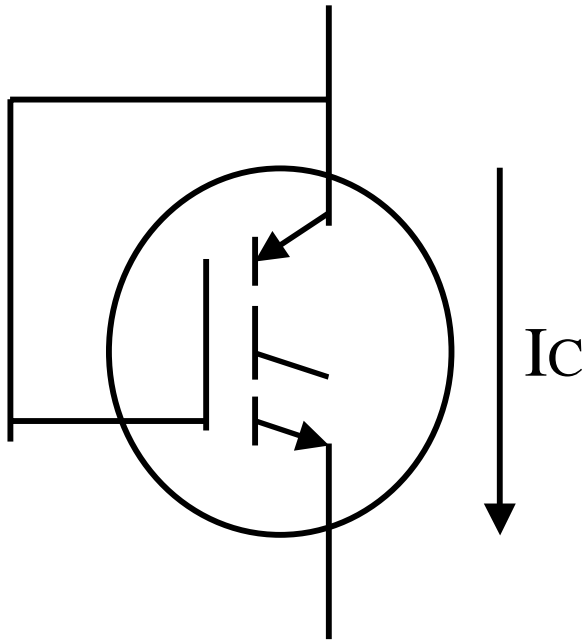


FIGURE 4.1
IGBT in V_{CEON} mode.

resulting in a current imbalance. This imbalance is unavoidable. However, it can be reduced to tolerable level with proper techniques. Two of these techniques are described as follows:

- Select IGBT chips that are physically next to each other in the wafer. This is simple and often works, but there is no guarantee because side-by-side chips may or may not always conform to the tight tolerance required.
- Select IGBT chips with closely matched V_{CEON}s for the diode-mode voltage.¹⁻³ V_{CEON} of the IGBT is obtained by shorting the gate with the collector and then measuring the voltage across the emitter and the combined terminal at a certain current level. This current must be performed in pulse condition to avoid any device self-heating.

Based on these measurements, the IGBT chips can now be sorted into two, three, or four groups with V_{CEON} or ΔV_{CEON} variation of less than, say, 0.30, 0.20, 0.15, or 0.10 V within each group. The chips from each group can then be paired with the approximate current imbalance shown in [Table 4.1](#).

TABLE 4.1Percent Current Imbalance vs. ΔV_{CEON}

ΔV_{CEON} (V)	Current Imbalance (%)
0.30	15
0.20	10
0.15	7.5
0.10	5

The current imbalance should be limited to 15% maximum.

It is practically impossible to measure the V_{CEON} of the IGBT at 200 A in chip form. One approach is to measure the V_{CEON} at low current (1 to 5A) and then extrapolate to 200A. This would require using a probe station with special tungsten probe tips that can handle several amperes of current. The IGBT wafers can be probed and mapped. The data can be stored in disc. This may be done by the module manufacturer or IGBT chip supplier (see [Section 4.1.5](#)). The grouping at automatic chip attachment is based solely on this mapping. The following is a list of possible suppliers of the probe station:

- Wentworth
- Karl Suss, Inc.
- Electroglas

Sorting is necessary for IGBT with punch-through (PT) structure, which has a negative temperature coefficient for V_{CEON} . For NPT IGBT, with its positive temperature coefficient, sorting is less crucial.

4.1.1.2 Junction Temperature Imbalance

Any current imbalance will lead to different junction temperatures. In the case of parallel operation, the chip that carries more current has a higher junction temperature, which may exceed the maximum-rated 150°C. Because the reliability factor varies inversely with the junction temperature in an exponential manner, this temperature imbalance becomes a major concern.

Thermal coupling is the key to reducing junction temperature imbalance. If the thermal coupling between the two paralleled IGBT chips is good, the junction temperature differential can be greatly reduced. In the construction of the 200 A module, the two paralleled IGBT chips are assembled on two different ceramic substrates, which are then attached to the common metal base plate. A good thermal coupling between the two IGBT chips requires the following:

- Solder attachments with as few voids as possible
- Solder with good thermal conductivity (Sn/Ag, Sn/Ag/Cu)

- Ceramic substrate with good thermal conductivity (Al_2O_3 , AlN , Si_3N_4)
- Metal baseplate with good thermal conductivity (Cu , AlSiC)

Good solder attachments are crucial during manufacture and must be monitored constantly to reduce voids as much as possible.

4.1.2 Cleaning

Cleaning plays a major role in ensuring the reliability of the power IGBT module. Using the proper cleaning agent and equipment will help enhance the electronic quality and reliability of the module. To select and implement the correct cleaning system successfully, one must know the types of contaminants involved. One also must understand the environmental requirements, which are continually forcing the cleaning chemistry to be environmental friendly but still effective.⁴

During the process of manufacturing the power IGBT module, many possible contaminants can end up on the surface. Even though the degree of contamination depends on the production facility and the operator training, contaminants are ever present and can be broadly classified into three groups:

- Group 1: Particulate material
- Group 2: Polar/ionic
- Group 3: Nonpolar/nonionic

Table 4.2 summarizes these contaminants⁵ as applicable to power module process.

TABLE 4.2

Surface Contaminants

Group 1 Particulate Material	Group 2 Ionic/Polar	Group 3 Nonionic/Nonpolar
Metal or plastic chips	Flux activators and flux	Flux rosin
Dust	activator residue	Flux resin (refers to synthetic
Fibers	Soldering salts	resins)
Handling soils	Sodium and potassium	Oils
Lint	chlorides from	Grease
Insulation	fingerprints	Soldering soils
Hair/skin	Neutralizers	Handling soils
Solder balls	Ionic surfactants	Hand creams and lubricants
Other airborne matter	Residue from cleaning,	Silicones
	etching, and plating	Nonionic detergents or
	operations	surfactants
		Organic processing material

The particulate materials of group 1 typically require mechanical energy, such as ultrasonic, spray, or centrifugal, for their removal. Of these three techniques, ultrasonic is believed to be the most effective. Ultrasonic cleaning can remove particles down to 0.05 μm from the surfaces. It can clean parts with complex geometries because ultrasonic cavitations will occur anywhere the solvent–water medium can reach. Spray cleaning and centrifugal cleaning are more directional. A study shows that ultrasonic cleaning is 5 to 15 times more effective than spray-only cleaning.⁶

However, in metal base-plate cleaning, the scrubbing action of the ultrasonic cavitations can cause the erosion of metallic surfaces if the intensity is high enough or if the time of exposure is long enough. Therefore, in actual applications, the following factors should be considered:⁵⁻⁷

- Choose 40-kHz frequency. The higher the frequency, the gentler the cavitations. High frequency removes small particles, and low frequency removes large particles. Sometimes it is necessary to use a range of multiple frequencies (up to 300 KHz if necessary) in rapid succession to achieve a thorough cleaning. The latest trend is to operate the ultrasonic tank at three or four different frequencies simultaneously.
- Use a power of about 30 W/l. Monitor the sonic power using one of the following:
 - Sonic meter probe, which will provide a general indication of overall energy level and its spatial distribution.
 - Sonoluminescence probe, which also indicates energy level and distribution or cavitation density in the cleaning fluid. A possible supplier is ProSys.
 - Aluminum-foil erosion test (this is a go/no-go test only).
- Lower the surface tension of the solvent by heating the solvent to about 45°C.
- Use a typical solvent-to-surfactant ratio, such as 9:1. Fluorochemical surfactants are more efficient than the hydrocarbon or silicone type.
- Use sweep frequency generators to smooth the distribution of energy within the tank. Check the distribution with a sonic meter probe. Minimize the time of exposure to about 3 to 5 min.

Group 2 and group 3 contaminants can mostly be removed by wet chemistry. The standard method is to use a suitable cleaning medium in either a batch cleaning or an in-line cleaning machine. This medium should be capable of extracting or removing the contaminants from the surface and should also be a non-ozone-depleting type of chemical. The following is a list of its desired properties:

- Has a surface tension less than 20 dynes/cm
- Does not attack silicon or IGBT/FRED chips
- Does not attack metal such as Cu, Al, Ni, Ag, Sn, Rb, Bi
- Does not attack solder such as Sn/Ag, Sn/Ag/Cu, Pb/Sn
- Does not attack ceramic substrate
- Is effective in removing group 2 and group 3 contaminants
- Has cleaning chemistry flexibility, either by spraying, ultrasonic immersion, or vapor phase system; is easily recyclable
- Leaves zero residue on clean surfaces
- Leaves no ionic contamination after rinse
- Does not create galvanic cell
- Provides high solderability yield
- Produces no hazardous fumes for operator, no HAP, high vapor density
- Produces no environmental problem; is “green,” non-ozone depleting, SNAP approved, easily disposable
- Is a mature technology
- Is cost effective: less than \$5/lb

There are three methods in wet cleaning:

- Aqueous cleaning
- Semiaqueous cleaning
- Solvent cleaning

4.1.2.1 Aqueous Cleaning

Aqueous cleaning uses water only as the cleaning medium or water with additives that make up less than 50% of the total composition. Water is quite effective in removing ionic/polar materials but requires additives, such as saponification agents, to treat nonionic/nonpolar residues.

Aqueous cleaning has the advantages of being nonflammable and environmentally and operator friendly. However, it is not effective in penetrating tight spacing (< 10 mil). The coming of Pb-free solders may present a challenge for aqueous cleaning. Pb-free solders require a more aggressive flux formulation than that of the conventional Pb-based solder. With higher reflow temperature, their residue will be darker and more intense, and therefore more difficult to remove, which may require modifications to existing aqueous chemistry.

Aqueous cleaning is usually a three-step process:

1. **Clean or wash** — Ultrasonic, spray, or centrifugal wash in water with various additives, depending on the cleaning technique used.
2. **Drag out/rinse** — Ultrasonic spray, or centrifugal rinse in hot DI water followed by hot DI water overflow rinse (¥ 2). Sometimes, an additional neutralizing step is also included if a strong alkaline agent is used.
3. **Dry** — High-purity hot air knife blows off at about 110°C or hot air circulatory or centrifuge dry, followed by convection at about 150°C, infrared/convection, or vacuum drying sections. Water drying is very energy intensive.

The cleaning can be done either in batches for small volumes or by an automated in-line system for high volumes. A water evaporator/recycler is generally used to filter out the soluble contaminants and recycle the water. Most systems can be operated in either open- or closed-loop configuration. During cleaning, the parts should be positioned separately from each other to avoid any incomplete cleaning or damage by contact.

4.1.2.2 *Semiaqueous Cleaning*

Semiaqueous cleaning is a solvent-clean/water-rinse process. Like aqueous cleaning, it has three key steps:

1. **Clean or wash** — Ultrasonic, spray, or centrifugal immersion wash in solvent. Here, the typical cleaning solvents are:

Organic

Non-ozone depleting

Low in vapor pressure, with flash point in excess of 38°C

Flammable

Low in volatility; low in viscosity

Long in bath life

They can be broadly classified into two categories:

Water-soluble, non-terpene-based, polar organic solvents such as heavy alcohols, glycol ethers, and cyclic amines. Because they are water soluble, they can be easily removed during rinsing, and entrapment is not an issue. The difficulty lies in the treatment of the rinse water containing the solvents, the saponifier, and the dissolved contaminants. Again, an evaporator/recycler is required for recycling.

Water-insoluble, terpene-based organic solvents such as terpene, aliphatic hydrocarbons, and synthetic alcohols. Because they are

water insoluble, they require mechanical energy, such as ultrasonic, spray, or centrifugal, for removal, and entrapment may be an issue. The advantage is the ability to separate the solvents from rinsing water, thus allowing the solvents to be recycled back into the wash section for reuse.

2. **Dragout/rinse** — Ultrasonic, spray, or centrifugal rinse in hot DI water followed by hot DI water overflow rinse ($\times 2$). If the solvents are to be recycled, there is an additional emulsion rinse stage fitted with a decanter for separating the solvents from water. Because water requires high energy input for drying, the current trend is toward a cosolvent process, namely, to use another solvent as a rinsing agent instead of water. This solvent is different from the cleaning solvent. Possible candidates are:

PFC (per fluorinated compound)

HFC (hydrofluorocarbon)

HFE (hydrofluoroether)

Note: Strictly speaking, cosolvent cleaning is a solvent cleaning process.

3. **Dry** — High-purity hot air knife or hot air recirculating through HEPA filter or centrifuge dry, followed by conveyORIZED convection, infrared/convection, or vacuum drying section.

Because semiaqueous cleaning solvents are flammable, all equipment and tools must be able to handle such materials. Avoid solvent mist. The cleaning area must also be well ventilated or equipped with a fume-extracting system.

4.1.2.3 *Solvent Cleaning*

Solvent cleaning involves the following steps:

1. **Preclean** with hot solvent vapor.
2. **Clean** or wash in distilled solvent with or without ultrasonics or spray agitation.
3. **Rinse** in hot solvent vapor.
4. **Dry** by solvent boiling and solvent recycle.
5. **Vacuum** dry.

If step 2 is skipped, then this becomes the common vapor degrease process. Because water is absent from the entire process, drying is much less energy intensive: about 40% less than aqueous or semiaqueous. Most of the solvent cleaning systems use the same solvent for both cleaning and rinsing, although cosolvent systems are also available. Solvent cleaning is simple and

effective, including for tight spacing circuitry. The major concerns are fumes, handling, and disposal. The high cost of some solvents may also be an issue.

In general, the popular solvents currently used are of the HFC or HFE type.^{5,7-9} These are “green” or non-ozone depleting, nonflammable, and nonpolar, with properties similar to CFC-113. The EPA and SNAP have banned the usage of CFC-113, all solvents containing 1,1,1-trichloroethane, and most HCFC, such as HCFC-141b, but still approve HCFC-225, which is a very low ozone-depleting material. Low-flashpoint polar solvents, such as isopropyl alcohol (IPA), cyclohexane, and acetone, are also commonly used.

Some of the cleaning solvents are:

- DMPD, or dimethyl-2-piperidone by DuPont — This is an isomeric solvent blend consisting of 1,3- and 5-dimethyl-2-piperidone. It is a colorless, high-boiling liquid with a mild odor. It has high chemical stability, good solvency, and low toxicity. It is flexible in its cleaning chemistry and can be used in either the solvent or the semiaqueous mode.
- AK-225 by Asahi Glass — Even though it is HCFC, it is SNAP approved, VOC exempt, and nonflammable. It may, however, attack plastic parts.
- n-propyl bromide (nPB) — This nonflammable material has a very low ODP of 0.013 and has properties similar to 1,1,1-trichloroethane. It is recommended by SNAP as long as the exposure limit is 25 ppm and a purity specification of < 0.05% isopropyl bromide is met.
- HFE-7100, -7200, and -72DE — All are listed as acceptable substitutes for HCFC-141b.
- HFC-43 — This solvent has 0 ODP and is good for tight spacing circuitry.
- Vertrel by Miller-Stephenson — Its boiling point, surface tension, and viscosity are comparable with those of CFC-113.
- Because most of the solvents are nonpolar, the latest cleaner is of the bipolar-solvent composition, combining polar and nonpolar solvents that can remove both polar and nonpolar contaminations in one step. These bipolar-solvents also nonflammable. Typical composition is 93/7. Examples are:
 - HFE/IPA azeotrope
 - HFC/IPA azeotrope
 - nPB/IPA azeotrope

The following are possible suppliers of azeotrope solvent:

- DuPont
- 3M

TABLE 4.3

Comparison of Solvents

	Cost (\$/lb)	Karui- Butanol value (KB)	Vapor Density (Air = 1)	Surface Tension (dyne/cm)	HAP (Hazardous Air Pollutants)	Flash Point
n-propyl bromide	4	125	4.25	25.3	None	None
AK-225	13	41	7	16.8	None	None
HFC (Vertral)	19	9.4	7.86	15.1	None	None
HFE-71PA	19	10	7.51	14.5	None	None
Isopropyl alcohol	1	—	2.1	21.7	None	0.60

To select the proper cleaning solvent, check the solvent's solubility parameter (Kauri-Butanol value), which indicates the degree of solubility for organic materials. Solvency curves are also available for a large number of solvents.

Note that higher KB-value solvents are good for heavy organics, oil, and grease; lower KB value solvents are for light organics and particle removal. The heavier the vapor, the more contained is the solvent in the equipment; the lower the surface tension, the better is the wetting. All solvents have no emission of hazardous air pollutants. IPA has a low flashpoint and must be used in special equipment for handling flammable solvents.

The following is a list of possible suppliers of cleaning systems:

- Aqueous cleaning:
 - Forward Technology Industries
 - Branson Ultrasonics Corp.
 - General Product Devices
 - Austin American Technology Corp.
 - Aqueous Technologies
- Semiaqueous cleaning:
 - Forward Technology Industries
 - Vitronics
 - Austin American Technology Corp.
- Solvent cleaning:
 - Forward Technology Industries
 - Branson Ultrasonics Corp.
 - Austin American Technology Corp.
 - AMA Universal — hermetically sealed system
 - Tiyoda-Screc — vacuum degreasing system

4.1.2.4 Key Cleaning Steps for Power Module

In the manufacturing of the power IGBT module, there are three key cleaning steps: presolder cleaning of the parts,⁸ postsolder cleaning of the assembly, and pre-wire-bond cleaning.

4.1.2.4.1 Presolder Cleaning of the Parts

This involves the following operations on the parts:

- Cleaning/degreasing
- Rinsing
- Drying
- UV cleaning
- Vacuum baking

Any of the three wet-cleaning chemistries can be used. Each chemistry has advantages and disadvantages, and the selection will depend on the contaminants to be removed. In most cases, ultrasonic aqueous cleaning with a saponifier or standard aqueous cleaning chemical should be adequate. However, care must be taken to make sure that the cleaning chemical is compatible with the cleaning technique. For ultrasonics, use a high foaming type.

The following are possible suppliers for aqueous cleaning chemicals:

- JNJ Industries
- Aqueous Technologies

Power IGBT/FRED chips do not require cleaning. The wafers are processed in a cleanroom, cut, and left on sticky film, then packaged and shipped in antistatic, airtight bags filled with dry N₂. Before usage, they should be stored in antistatic, class-1000 controlled environment cabinets. The bags should be opened only inside the laminar hood or modular clean room unit.

Due to the stubborn nature of some of the group 2 and group 3 contaminants, it is often necessary to subject the parts, especially ceramic substrates, to an additional UV clean¹⁰ or a CO₂-based dry cleaning.

- UV Clean — By placing the cleaned/degreased parts within 5 mm of an ozone-producing UV source, such as a mercury or xenon lamp, a near-atomically clean surface can be achieved in 1 min. Ozone has an ionization potential of 2.1 and is very effective in breaking down bonds of contamination.
- An alternative to the UV clean is CO₂-based dry cleaning. This process will be discussed in [Section 4.1.2.5](#).

The following is a list of possible suppliers of UV cleaner:

- American Ultraviolet
- Jelight
- Xenon

The final step for presolder cleaning is a high-temperature vacuum bake.⁸ The vacuum bake at 150°C for 4 to 8 hours will ensure a dry surface before soldering. The vacuum should be maintained at 50 μm of mercury. After baking, the oven should be back-filled with ultradry nitrogen. Vacuum bake is critical in trying to achieve void-free power-chip attachment.

4.1.2.4.2 *Postsolder Cleaning of the Subassembly*

The subassembly should be cleaned within 1 hour after reflow. Again, any of the three cleaning chemistries can be used here, with the choice depending on the types of flux and contaminants being removed. In general, both semiaqueous and solvent cleaning, especially azeotrope, are very effective in treating rosin, low-solid, and synthetic-activated flux residues. For post-wire-bond assembly, heavy mechanical energy input should be avoided because this may weaken or break the wire bonds. Here, solvent cleaning is the preferred method. The parts may be cleaned in the solvent without ultrasonics or spray agitation, rinsed in hot solvent vapor, and dried by solvent evaporation or vacuum bake.

4.1.2.4.3 *Pre-Wire-Bond Cleaning*

Plasma cleaning,^{8,11} is a dry process, typically performed in an argon gas plasma for about 5 min. under the RF power of 50 to 75 W and a gas flow of about 2 to 5 cc/min.

The following is a list of possible plasma cleaner suppliers:

- March Instruments
- Technica Plasma
- Plasmatech

4.1.2.4.4 *Other Cleaning Steps*

- Any wet spillover from silicone gel/epoxy coating or case/cover epoxy attachment must also be cleaned. This is usually done by a clean, soft, and lint-free wipe. *Do not use solvent.*
- Manual soldering of fast-on tabs and any repair or rework should also be followed by cleaning, such as CO₂-based dry cleaning or vapor degrease.
- Any excess solder paste from the edges of the substrate should be removed by a clean, dry swab. *Do not use solvent.*

Note:

- All cleaning must be performed in a controlled environment.
- After cleaning, the parts should be transported via a minienvironment container to an assembly area of a controlled environment.

4.1.2.5 New Dry-Cleaning Method

In addition to the previous conventional wet-cleaning methods, the latest introduction that proves to be quite effective is the CO_2 *jet-spraying technique*, also called *snow-cleaning* or *cold-cleaning*.^{8,12} In this cleaning, a jet of solid CO_2 snow and gaseous CO_2 impinge on the surface to dislodge and sweep away contaminants. It is effective in removing mechanically bonded and nonpolar contaminants. Snow cleaning is a relatively new process developed as an alternative to using CFC and other organic solvents, which are environmentally damaging. It serves to supplement or replace spray cleaners, vapor degreasers/dryers, and ultrasonic cleaning systems.

Benefits of using snow cleaning are the following:

- Requires no solvents or water
- Is a dry process
- Removes submicron particulates
- Can remove films of grease and oils
- Cleans rapidly, in seconds
- Can be used on IGBT and FRED chips
- Can be used for post-wire-bond cleaning
- Is easy to set up and can be used on small volume lots, such as post rework

This cleaning must be performed in a dry, inert atmosphere to avoid moisture condensation on the chip surfaces.

The equipment for snow cleaning is relatively inexpensive. Cylinders of pressurized CO_2 and a variety of handheld automated spray guns are commercially available. The velocity, size, and density of the snowflakes can be controlled to provide intensive, moderate, or mild cleaning. Care must be exercised to make sure that the CO_2 is clean.

The following is a list of possible CO_2 jet-spraying equipment suppliers:

- Eco-Snow Systems
- Tomco Equipment
- Applied Surface Technologies
- Alphasus Cleaning Technologies

4.1.2.6 *Level of Cleanliness*

Inadequate cleaning can lead to catastrophic device failures. However, excessive cleaning can lead to costly products. An optimal level of cleanliness is desirable.^{13,14} J-STD-001 and IPC-6012 outline the cleanliness level for different residue types. To achieve this level, one must be able to measure or test the cleanliness and then correlate with life test results. These measured data will also assist in deciding which cleaning chemistry to use.

There are two approaches to assess or measure^{5,6,8,15–17} the level of cleanliness: coarse testing and analytical testing.

4.1.2.6.1 *Coarse Testing*

Coarse tests do not measure the actual surface cleanliness or identify the species of contaminants. They do provide a general indication of the level of surface cleanliness. The following tests can be used as a continuous in-line process monitor:

- Particle counting — The area or surface of interest is flushed with a solvent and the solvent is analyzed using a laser-particle counting system.
- Magnified visual inspection.
- Water break test.
- Contact angle measurement.
- Solvent extract conductivity.

[Table 4.4](#) shows a list of coarse testing techniques.

The following are possible suppliers of systems for monitoring cleanliness:

- Particle Measuring Systems, Inc. — Surfex
- AST Products, Inc. — Contact Angle System
- Aqueous Technologies — Ionic Contamination Tester

4.1.2.6.2 *Analytical Testing*

Analytical tests provide detailed, specific information about the amount and species of contaminants. Analytical tests are expensive and time consuming, are normally done on a periodic basis, and are useful for failure analysis.

[Table 4.5](#) lists in-depth techniques for analyzing surface cleanliness.

MCNC Analytical Lab is a possible supplier that provides analytical testing services.

4.1.3 *Solder Attachment*

The power IGBT/FRED chips, the terminals, the ceramic substrates, and the metal baseplate are bonded together by solder. As discussed in [Chapter 3](#),

TABLE 4.4**Coarse Testing Techniques for Cleanliness**

Technique	Description
Particle counting	Provides general information about the level of surface cleanliness Does not measure the actual surface cleanliness Does not identify species of contaminants Simple, effective — can be used for in-line monitoring and an early warning
Magnified visual inspection	Can be used for in-line monitoring Provides a measurement of occurrence of soil or particulates present directly on the surface Provides an absolute or relative measure of some surface characteristics that relate to the level of surface cleanliness
Water break test	Estimates cleanliness by estimating the wettability of a surface — a clean surface can maintain an unbroken layer of water for at least 1 min. when positioned vertically Is simple and reproducible Can be used for in-line monitoring Provides an absolute or relative measure of surface cleanliness Does not identify species of contaminants Is most effective in detecting organic or oily contaminants
Optically stimulated electron emission (OSEE)	Estimates the presence and thickness of thin films on a surface from the rate of change in emitted electrons from a surface exposed to UV light Provides an absolute or relative measure of surface cleanliness Does not identify the species of contaminants Does not require a polished surface Does not detect particulates
Fluorescent dye test	Detects oil film that will absorb fluorescent dyes and illuminate when exposed to UV light Is a destructive test
Contact angle measurement	Estimates cleanliness by measuring the contact angle of a liquid drop on the surface Is simple and reproducible Can be used for in-line monitoring Does not identify species of contaminants
Solvent extract conductivity	Measures the amount of ionic material removed from the surface; test is performed at 45°C, with typical test time of less than 15 min Does not identify the species of contaminants Can be used for continuous in-line monitoring Conforms to IPC-JSTD-001
Surface insulation resistance	Uses surface resistance as a gauge of cleanliness Does not identify the species of contaminants Is suitable for initial process qualification Conforms to IPC-TM-650, method 2.6.3

TABLE 4.5**Analytical Testing Technique for Cleanliness**

Technique	Description
Secondary ion mass spectroscopy	Accurate molecular weight impurity detection; good for detection of trace amounts of gases and low molecular weight organics Benchtop SIMS system available from Ametek
Gas chromatography (GC)	Quantitative analysis of volatile organics Very efficient technique Benchtop, miniaturized, and high speed GC unit available from Photovac; the latest trend is toward a combined GC-SIMS system
Scanning electron microscopy (SEM)	High magnification (300,000×) with large depth of focus obtained Used for magnifying abnormalities during failure analysis
Energy dispersive x-ray analysis	X-ray spectrum of chemical elements near the surface can be analyzed simultaneously
Auger electron spectroscopy	Investigates small depths of subsurface (4–15 Å). Can detect low levels of elements (0.1%) in a small area (< 1 µm ²)
Infrared spectroscopy	Provides identification of organic functional groups Detects impurities
Electron spectroscopy for chemical analysis	Detects low levels of elements (0.1%) but with better repeatability than Auger
Rutherford backscattering spectrometry	Detects impurities in substrate material and provides information on the atomic mass of the impurity
Laser ionization mass spectrometry	Uses a laser pulse to ionize the sample Performs similar function to SIMS
Focused electron beam-induced current	Can detect opens or shorts in metallization

the solders used are usually Sn/Ag/Cu or Pb/Sn types. These can be in the form of preform or paste, which is applied by dispensing or screen-printing.

The common method for component attachment in IGBT module assembly is a two-solder process. Solder 1 is for the attachment of power chips to the ceramic substrate, whereas solder 2 is for attaching the terminals/connecting bridges to the ceramic substrate and the ceramic substrate to the metal base plate. Solder 1 has a melting temperature of about 25 to 40°C higher than solder 2.

- **Chip attachment** — This is usually done by an automatic chip placement machine located at the entrance of the reflow oven. After the chips are placed on the solder paste or preform, the substrates are moved automatically onto the conveyor belt of the reflow oven for soldering.

- Ceramic substrate, power terminal, connecting bridge attachment
— This is usually done manually by using one of the two following fixtures:
 - A graphite fixture in the shape of a block with detachable parts for the placement of base plate, ceramic substrate terminals, and bridges. Solder can be either screen-printed or dispensed onto the baseplate and ceramic substrate. Solder preform can also be used. If necessary, graphite weights can be placed on top to ensure good soldering. The material used is semiconductor-grade graphite, such as Poco graphite.
 - A graphite fixture with alignment sheets. Here, the fixture is a flat graphite plate about 10 mm thick with guided pins that are in line with the mounting holes of the baseplate and the sheets. The sheets or frames are metallic, usually stainless steel of 1 to 4 mm thick, and have windows etched out for the placement of different components. The guided pins are designed with stops to control the height of these sheets above the base plate. Again, graphite weights or spring clips can be used to ensure good soldering.

Poco Graphite, Inc., is a possible supplier of custom-designed graphite fixtures.

The two-solder process is simple and straightforward but may present some difficulties at rework after the second soldering, due to the presence of the bulky power terminals. To overcome this, some OEMs have used a third solder for attaching the terminal/bridge to the ceramic substrate. This becomes a three-solder process, with each soldering step 25 to 40°C lower than the preceding one. This approach is more complex and also requires higher-temperature soldering for the power chip attachment, usually of high Pb content, such as Pb/Sn/Ag, with reflow temperature at or over 300°C. In this approach, both the power chips and the completed ceramic substrate can be attached by an automated placement machine.

The most widely used equipment for solder attachment is a conveyor-belt reflow oven, such as the forced-air convection type, the infrared (IR) type, or a combination of both. These types^{5,18–20} have been used for high-volume production. However, there are some drawbacks to these systems. One of the main problems is heating uniformity. With the IR oven, the source of heat is at a much higher temperature than the modules being heated. Hence, the temperature distribution over the module depends largely on its local properties, such as thermal conductivity and thermal loading. The forced-air convection oven has the potential to solve this problem. In this process, the source of heat is the heated gas (typically nitrogen),²¹ the temperature of which is controlled to be slightly above the desired module temperature. In this manner, the process is quasi-equilibrium, which ensures uniform temperature distribution regardless of variations in the module's local properties.

The higher the flow rate of forced convection, the more effective is the heat transfer coefficient between the modules and the hot gas.

A forced-air convection reflow oven is arranged into zones similar to those of the IR type. A continuously moving conveyor is loaded with modules so that every zone is filled. However, continuous motion of the conveyor permits no possibility of separating zones with barriers of some kind. Although this poses no problems in IR reflow ovens (because mixing between zones could occur only by the inefficient process of diffusion), in forced-air convection ovens gases in adjacent zones are mixed by the process of convection. Zone mixing is detrimental to the reflow process because it results in a change of the established or desired reflow profile. Various techniques are being used to reduce zone mixing.^{22,23} These techniques rely on different ways of directing and manipulating gas flow in each zone. As a result, forced-air convection ovens tend to be large, complicated, and expensive.

Other solder reflow techniques, such as conduction, hot gas, or laser, are being used mostly in rework operations, not for primary attachment. Vapor phase reflow is used strictly in high-volume production, such as Printed Circuit Board (PCB), to compensate for its high operating cost.

With the advent of Pb-free soldering, flux management becomes significant. The latest reflow oven is equipped with a self-cleaning flux extraction system that is claimed to reduce maintenance intervals by 50 to 75%.

The following list contains some useful information about soldering operations for IGBT modules:

- Because IGBT is a MOS-type device, extra caution must be exercised against ESD. All operators must be grounded. All equipments must be grounded. All grounding connections must be monitored. Loading areas should be sprayed with deionizer. All cabinets, storage, and walking areas must be static free. Temperature should be maintained at 20°C with RH at 40 to 60%.
- All loading (attachment) operations must be performed in a controlled environment, such as a laminar hood. The components are relatively large. To achieve a void-free attachment, all dirt, dust, and airborne matter must be reduced to minimum.
- Because some of the operation is manual, all operators must wear gloves or finger cots. A vacuum pencil or suction lifter should be used to pick up components.
- Oven loading should be preceded and followed by a pair of unloaded fixtures.
- Spacing between fixtures is usually about the length of the fixture.
- Oven unloading should be preceded by a controlled cooling zone.
- Because this is a bare chip-and-wire assembly, *avoid soldering with flux if possible*. Optimize cleaning and reflow techniques — perhaps

use vacuum soldering — to achieve good-quality attachment. Reflowing in a reducing atmosphere, such as hydrogen with less than 2 ppm O₂, is another alternative that replaces the usage of flux. This process, however, is more effective with higher-temperature (> 300°C) solderings, such as those of the higher Pb content. The oxygen level should be closely monitored for safety purposes.

4.1.3.1 Single-Chamber/Vacuum Soldering

For relatively low-volume production, the single-chamber oven assembly may be a viable alternative approach. In the single-chamber oven assembly, there is no conveyor belt, and the IGBT module assembly experiences the heating cycle via changing temperatures in the single-chamber oven. In other words, the whole chamber goes through the same heating cycle as the IGBT module assembly. The chamber itself is sealed and airtight, with negligible gas leakage. A single-chamber oven also permits vacuum soldering, which has shown promise for void-free chip assembly.²⁴

Single-chamber oven assembly offers many benefits, such as the following:

- Very uniform heating (as compared with the infrared type)
- No cross-zone mixing (as compared with the forced-air convection type)
- Precise and constant reflow profile
- Low consumption of gas (typically nitrogen)
- Gas with a controllable level of oxygen (< 20 ppm), as compared with forced-air convection and IR types, both of which have two open ends
- Possible void-free solder attachment in vacuum environment
- Possible flux-free soldering in vacuum environment and use of solder preform instead of paste

Table 4.6 compares the forced-air convection, the IR, and the single-chamber oven assemblies.^{5,18}

The following is a list of possible single-chamber oven vacuum reflow furnace suppliers:

- Rehm
- ATV Technology, Inc.:
 - Single Vacuum Chamber
 - In-line conduction (hotplate) vacuum reflow
- Sierra Therm Vacuum Products Group

TABLE 4.6

A Comparison of Different Reflow Methods

	Forced-Air Convection	Infrared	Single Chamber
Heating	Uniform	Nonuniform	Uniform
Efficiency	Poor	Good	Good
Zone mixing	Some	None	None
Gas consumption	High	High	Low
Gas purity	Reasonable	Reasonable	High
Reflow profile	Can vary	Good control	Precise constant
Vacuum soldering	Not possible	Not possible	Possible
Capacity	High volume	High volume	Low volume
Dimension	Large	Varies according to capacity	Small
Solder	With flux	With flux	Without flux in vacuum

In the reflow process, the solder and the components are exposed to a heating process, which is represented by a reflow profile, in a gas environment. This reflow profile and the processing gas used have a direct bearing on process yield, solder joint integrity, microstructure, and reliability of the modules. Therefore, two keys issues are:

- Reflow profile
- Processing gas

4.1.3.2 Reflow Profile^{5,25}

The critical parameters of a reflow profile are:

- Preheat time
- Preheat temperature
- Time of solder above liquidus
- Initial ramp rate
- Cooling rate

Figure 4.2 shows a typical ramp/soak/spike reflow profile for the 63Sn/37Pb solder.

The following discussion presents a guideline for establishing these profile parameters. It must be emphasized that the ideal reflow profile is different

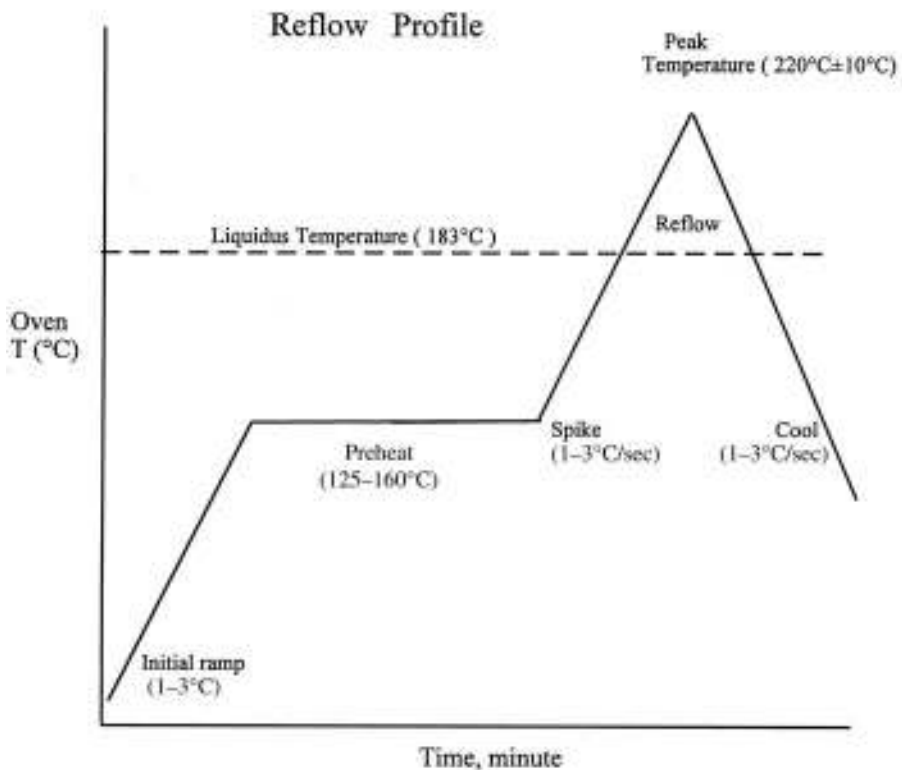


FIGURE 4.2

A ramp/soak/spike reflow profile for a 63Sn/37Pb solder.

for each production facility. It depends on many factors, such as those listed here:

- Reflow equipment used
- Reflow soldering method
- Solder used
- Processing gas
- Product

The best time-temperature profile for the product must be established in each case.

Useful information can be found at *IPC Roadmap, a Guide for Assembly of Lead-Free Electronics* (see www.leadfree.org and www.ipc.org).

4.1.3.2.1 *Preheat Soak Time and Temperature*

The main purpose of the preheat or soak time and temperature is to ensure that all components on the substrates are heated evenly before the reflow spike begins. Large temperature differences across a substrate can result in the failure of portions of the substrate to reach reflow temperature simultaneously, thereby causing uneven soldering. These temperature differences and their resultant problems can impair long-term solder joint integrity.

Preheat time and temperature are also critical to flux activation. If the time or temperature is set too low, the flux cannot clean the joints to be soldered, resulting in cold solder joints. On the other hand, if the time or temperature is set too high, the flux will evaporate, resulting in oxidation of the joints of poor wetting ability. Typical preheat temperatures for Sn/Pb solder range between 125 and 170°C. Preheat time is the time required to heat all components on the substrate to the same temperature and is dependent on the module size. It can vary between 0 and 120 sec. For Pb-free solders (such as Sn/Ag, Sn/Ag/Cu, or Sn/Cu), the preheat temperature should be raised to 170 to 190°C if the flux can accommodate the high thermal level. Some manufacturers have used a two-stage preheat profile for Pb-free solders.

4.1.3.2.2 *Time above Liquidus*

Time above liquidus influences the metallurgical properties of the solder joint. If the time is too low, it causes cold solder joints, poor wetting, and incomplete joints. If too high, it causes excessive grain growth and the formation of intermetallics. Both of these result in a weakened solder joint. Typical values are 20 to 90 sec. For Pb-free alloys, the time above liquidus is generally longer to promote the wetting and the spreading of the solder on the attachment pad.

4.1.3.2.3 *Peak Temperatures*

If peak temperature is set too high, damage to components — especially plastic components — and excessive warpage or delamination of the substrate may occur. If peak temperature is set too low, cold solders, poor wetting, and opens may occur. Typical values are 20 to 40°C above the solder melting point. For consistency, eutectic solders or solders with a narrow plastic region are preferred.

4.1.3.2.4 *Initial Ramp Rate*

The object of the ramp rate is to heat the module from room temperature as quickly as possible while achieving two particular goals. The ramp up should not be so rapid that it causes damage to either the substrate or the components. Also, it should not induce explosive elimination of the flux solvent. Typical ramp rates are in the region of 1 to 3°C/sec.

4.1.3.2.5 Cooling Rate

The ideal cooling rate should be a mirror image of the reflow ramp rate. The closer it is to the reflow ramp, the tighter the grain structure of the solder joint will be upon reaching its solid state, resulting in a solder joint of higher quality and bonding integrity. Experimental evidence indicates that a more rapid ramp and cool rate (2.5°C/sec) results in a finer grain size, which is considered preferable from the standpoint of solder joint life. Creep resistance, shear strength, and fatigue resistance are factors that may be affected by the cooling rate. For Pb-free solder, controlled cooling, such as multiple-zone cooling, is essential.

Table 4.7 shows typical parameter values of the ramp/soak/spike reflow profile for Pb and Pb-free solders.

The other commonly used reflow profile is the ramp-to-spike, or triangle, profile. Here, the initial ramp and the preheat zones are replaced by a single, slower ramp zone over the entirety. The ramp rate is about 1°C/sec. The results are less stress induced during soldering and lower energy cost, as compared to the ramp/soak/spike profile. Table 4.8 shows the relationship between reflow profile parameters and solder joint defects.

After the optimal profile has been established (after trouble-shooting from the symptoms listed above), it is crucial to maintain that profile. This requires the service of a thermal manager.^{26,27} *The installation of a real-time, continuous thermal manager on the reflow oven is critical to long-term solder joint reliability.*

An automated thermal manager can obtain real-time, live data output from a process that has traditionally been difficult to monitor. Using 30 thermocouples embedded in two probes mounted just below or above the conveyor, a thermal manager can monitor process temperature at the belt rather than at the heater element.

These temperatures are ideally displayed as process profiles on the video screen. A thermal manager can provide dynamic feedback, based on the set-up of the ovens, to verify that the process has been set up properly and falls within the ranges established for the reflow profile of a given assembly. During processing, a thermal manager can detect process temperature variations that oven-controlled thermocouples cannot detect and can reveal

TABLE 4.7

Typical Parameter Values of the Ramp/Soak/Spike Reflows Profile

	Pb/Sn	Sn/Ag/Cu	Sn/Ag
Preheat time and temperature	30–90 sec 150–170°C	60 sec 150–190°C (can be two stages)	60 sec 150–190°C (can be two stages)
Time above liquidus	30–60 sec	60–90 sec	60–90 sec
Peak temperature	215–220°C	235–255°C	240–290°C
Ramp/cool rate	0–2°C/sec	0–2.5°C/sec	0–2°C/sec

TABLE 4.8Reflow Profile Parameters vs. Potential Solder Joint Defects^{25,26}

Parameter	Character	Potential Solder Defects
Initial ramp rate	Too rapid rise	Cracked components Solder balls
Preheat time	Too little time	Poor flux activation Poor wet-out of solder Cold solder joints
	Too much time	Flux evaporation Flux deterioration Oxidation of solder
Preheat temperature	Too low temperature	Poor flux activation Poor wet-out solder
	Too high temperature	Flux evaporation Oxidation of solder
Peak temperature	Too low	Old solder joint (dull) Poor wetting of joint (void)
	Too high	Component damage Leaching
Cooling rate	Too slow	Larger grain size Intermetallics
	Too fast	Smaller grain size

these temperature drifts and their locations on the screen. Because this is a continuous monitoring process, the thermal manager creates a clear picture of trends and deviations, thus allowing potential problems to be detected quickly. At the same time, all data may be recorded permanently to the hard drive, enabling users to review process data from any previous production date.

The following is a list of possible suppliers of the thermal manager for reflow oven:

- KIC Thermal Profiling
- Data Paq
- Technology Information Corp.

4.1.3.3 Processing Gas

There are many disadvantages to conducting the reflow soldering process in an ambient air atmosphere. Air contains 21% oxygen; hence, it is an oxidizing atmosphere.

During reflow, the flux must provide protection to the active metal surface from oxidation. Otherwise, poor wetting will occur and reliability is questionable.

It is becoming common in the electronics industry to use high-purity nitrogen gas as the atmosphere during reflow.^{5,21,28} Nitrogen is an inert gas. If the parts-per-million level of oxygen is kept low (< 100 ppm), superior

TABLE 4.9

Effects of Nitrogen Purity on the Soldering Process

Description	Oxygen Level in Nitrogen Gas (ppm)
Reduction in discoloration	10,000
Less difficulty in cleaning flux residues	500
Reduction in solder ball formation	200
Reflow of low-residue solder paste	< 100

results are obtained during the solder reflow process. Further purification of nitrogen gas well beyond 100 ppm of oxygen is not necessary because field testing has shown that there is no difference in reflow quality for oxygen levels between 15 and 100 ppm. Table 4.9 shows the effects of nitrogen purity on the soldering process.

The increasing use of no-clean fluxes and pastes makes using nitrogen gas even more desirable. This is because the so-called no-clean fluxes and pastes all contain low solids. Hence, during soldering, they provide less protection than the regular fluxes and pastes.

The coming of Pb-free solder alloy also favors nitrogen gas. In general, Pb-free solder exhibits poorer wetting characteristics than Pb based solder. Nitrogen reflow would reduce the SnO content and improve the wetting.

Other advantages in using nitrogen as processing gas during soldering include the following:

- Less solder-ball formation
- Less difficulty in cleaning

The purity of nitrogen gas can also have an effect on other characteristics of the reflow soldering operation, such as:

- Wettability
- Wetting time/speed
- Spread flux
- Solder-ball formation
- Flux residue
- Microstructure of solder

Considering all these advantages of N₂ gas purity on reflow characteristics, it is worthwhile to install an N₂ gas analyzer and regulation system to control the oxygen level. One possible supplier of such a system is PBI Dansensor.

The major drawback of using controlled atmosphere soldering, such as nitrogen, is *cost*. (Typically, at 100 ft³, N₂ costs \$0.50 in the U.S., \$0.70 in

Europe, and \$1.10 in the Far East.) The higher the purity, the more expensive it is. As the pressure to reduce costs in the industry increases, the ultimate decision to use nitrogen should be based on a solid *cost-vs.-benefit* analysis that goes beyond the unit cost of nitrogen itself.

Several other issues concerning solder attachment must be addressed:

- Application
- Attachment of fast-on terminals
- Repair/rework

4.1.3.4 Application of Solder

Solder can be either preform or paste. Preform is cleaner but more expensive. On the other hand, paste needs to be thoroughly mixed and degassed.

Solder can be applied by stencil printing or dispensing within the pot life specified by suppliers.^{29,30} It is also conceivable that the solder can be pre-coated by making use of solder mask, a process similar to that used in the printed circuit board. Prerewflow solder integrity (uniformity, thickness, coverage, position) must be monitored carefully. (See [Section 4.2](#).)

Stencil printing has a clear-cut advantage of raw speed. However, the process is more involved. Its throughput and yield depend on the following factors:

- **Proper selection of solder paste** — Rheology, maximum particle diameter $\leq 1/5$ minimum aperture width.
- **Stencil thickness vs. aperture design** — Stencil thickness $\leq 2/3$ minimum aperture width.
- **Stencil aperture vs. land pattern** — Typically, aperture is 10 to 20% smaller than land pad.
- **Stencil material** — Ni-alloy, stainless steel.
- **Techniques in building stencils** — Chemical etching, laser, electro-formed.
- **Squeegee material** — Rubber, metal such as stainless steel.

Table 4.10 shows the pitch versus stencil thickness guideline.

TABLE 4.10

Guideline of Pitch vs. Stencil Thickness

Pitch Separation (mil)	Suggested Stencil Thickness (inches)
50	0.010
25	0.008
20	0.006

For reference, the following are processing conditions on stencil printing as suggested by a paste supplier:

- **Stencils** — Stainless steel stencils that are laser cut or chemically etched are recommended. Aspect ratio between stencil width and thickness should be 1:5. Area ratio between area of pad divided by area of aperture walls should be > 0.66 .
- **Squeegee** — Prefer stainless steel type. High durometer (80 to 90) rubber squeegees are acceptable.
- **Pressure** — 1.0 to 2.0 lb per inch of squeegee length is acceptable.
- **Speed** — 0.5 to 3.0" per second is acceptable.
- **Snap-off** — Printing on contact is preferred. Snap-off height of 0.010" is acceptable.
- **Environment** — 21–25°C, 35–70% RH. Keep airflow over the solder cream to a minimum to avoid evaporation.
- **Cleanup** — Use 6 to 9% isopropanol or saponifiers to clean stencils, squeegees, and related tools. For water-soluble solder creams, use warm water followed by an isopropanol rinse.

Note:

- Never reuse solder cream from stencil.
- Printing should be performed in a controlled environment.

Dispensing, on the other hand, is simpler and is more adaptable to component and height variations. The dispensing profile (dot size and height) depends on the rheology, viscosity, and wetting properties of the paste. For proper solder flow, a ratio of 1:7 must be maintained between the size of the solder sphere in the paste and the inside diameter of the dispensing needle. The most important factor is the correct proportion of the dot's diameter to its height. Low-viscosity materials should have a 3:1 diameter-to-height ratio, whereas high-viscosity pastes require a ratio of 2:1 or better. Where increased dot height is necessary, a higher viscosity paste is more suitable.

A good dot is

- Round
- Dome-shaped or with a "Hershey's Kiss" profile

A marginal dot is

- Oval
- Indented or flat profile

A poor dot is

- Splattering
- Stitching
- Tailing

To achieve consistency in dot shapes, the height distance between the needle and the substrate must be controlled accurately.

The pattern of the dispensed dots on the power-chip landing pad is preferred to be of a square or rectangular matrix. This will provide air paths for degassing during solder reflow. The dots can be 30 to 40 mils in diameter with 8 to 10 mils spacing, but these values can vary with different applications. The spacing between dots should be large enough for air passage but small enough to avoid creating voids. Other factors that must be considered are uniformity and average thickness of the reflow solder. It has been found that an *x-shaped dot* offers the greatest opportunity for air to be expelled from under the chips or substrates. X-pattern needles may be used for this application.

Solder paste designed for printing may or may not work as well in dispensing. Using solder paste not intended for dispensing may cause clogging of the dispenser. Dispensable or dispensing-grade solder paste must have a viscosity lower than that of traditional paste. Typically, dispensing-grade paste contains about 85% of metal content by weight, vs. 90% or higher for the printing grade.

The latest equipment is the *digital dispenser*, which can dispense precise dots. Dot diameter can be controlled down to 3 mil and placement accuracy to within 5 μm .

Creative Automation Co. is a possible supplier of digital dispensers.

4.1.3.5 Attachment of Fast-On Terminals

The fast-on terminals with precut wires are soldered manually by iron tip, laser, or heated gas to the copper metallization on the ceramic substrate. The process should be performed in an N_2 cover gas environment. The solder used can be of the Pb-free type, Sn/Ag, Sn/Ag/Cu, or Sn/Cu wire solder with 0.040" diameter.

When using iron-tip soldering, some useful practices are worth noting:

- Start at lower temperature.
- Select the bluntest and shortest tip possible to maximize heat-transfer efficiency. Use tips from reputable suppliers, such as Plato Products.
- Clean and trim the tip.
- Apply solder to the joint and not the tip.

- Avoid using flux, especially the water-soluble type, if possible. Otherwise, use the minimum amount of no-clean or RMA flux and heat-activate the excess residues on the substrate. Depending on the conditions, an additional CO₂ dry-clean or vapor degrease step can be implemented after soldering.
- Use a 30- to 60-W soldering iron and keep soldering time to less than 5 sec.

Heating-gas or microflame soldering offers some distinct advantages over tip soldering:

- Noncontact soldering
- Less thermal shock due to slower heating rate
- Temperature and heating rates are more controllable and repeatable

Even though the heating-gas system is more expensive than tip soldering, it is the preferred choice.

Note: Manual stations must be well ventilated or equipped with a fume-extraction system to avoid any possible health hazard, such as asthma, that can be caused by flux fumes.

The following is a list of possible suppliers of manual soldering stations:

- Pace, Inc. (tip soldering and N₂ cover gas)
- Leister Technologies (laser soldering or microflame soldering)
- Cooper Tools (digital soldering station and microsoldering pencil)

4.1.3.6 Repair/Rework

Rework is an efficient, cost-effective step in the total assembly process. It combines proper operator training (IPC- 7711, 7721) with the use of the right tools. Printing defects or mistakes before reflow can be corrected by simply removing the wet paste using a wiper soaked with DI water plus 6 to 9% semiconductor-grade isopropyl alcohol. Reworking defective components after reflow, however, requires a workstation capable of *heating the components until the solder underneath reaches liquidus without damaging or affecting the substrate and surrounding components.*

Three techniques are commonly used in repair/rework equipment: hot air, IR heating, and conduction.

4.1.3.6.1 Hot Air

One of the most common techniques is to use a hot-air nozzle that is large enough to envelope the defective component completely. The gas used is typically nitrogen so as to reduce oxidation on solder joints. The *low airflow system* is necessary because it eliminates the disruption of

adjacent components. The ability to adjust and control very low flow rates is essential. The air temperature is typically set at about 20°C above the solder melting point. After the preset heating time (4.5 min maximum), the solder melts and the vacuum sets in and removes the component. After the component is removed, the landing pads must be prepared for the replacement component. The residual solder is then removed by one of the following methods:

- Desoldering iron
- Desoldering hot gas system
- Desoldering braid (such as Soder-Wick, Fine-Braid, or desoldering ribbon by Plato)

Desoldering braid is the preferred method because it avoids damaging the pad. After the residual solder has been removed, the pad should be brushed and cleaned with an approved solvent to loosen any remaining flux, leaving the pad ready for application of new solder paste. Typically, a *lower-temperature solder paste* is applied onto the component pad by dispensing or single-component stencil printing. The rework equipment should then precisely mount a new component and reflow the solder to form an acceptable joint under N₂ coverage. The reflow process is computer controlled and should include all the different zones, as described earlier. The finished rework should be properly cleaned and visually inspected.

Key to both removal and replacement processes are the following:

- **Operator training** — Balancing temperatures and air flow, directing the air flow, shielding components, removing solder residue, cleaning the pad, dispensing new solder paste
- **An X-Y alignment system** — To ensure precision and repeatability of positioning
- **A tracking system** — To enable the replacement of the defective IGBT by a new IGBT that belongs to the same V_{CEON} group

The following is a list of possible suppliers for the hot-air rework station:

- Air-Vic Engineering Co.
- Pace, Inc.
- Advanced Techniques Co., Inc.
- OK International

4.1.3.6.2 IR Heating

An alternative to the hot-air process is the use of IR in the medium wavelength or “dark” range (2- to 8-μm wavelength). Dark IR guarantees uniform absorption and even heating across the entire surface of the components.

Unlike the hot-air system, the IR radiator has an X–Y aperture system, which can be adjusted for different sizes and shapes of the components. The IR radiation will be uniformly focused on the defective chips, with minimum effects on adjacent components situated as close as 0.5 mm. The IR system is more user friendly than the hot-air system.

The following are possible suppliers of the IR heating rework station:

- ERSa GmbH
- PDR SMT/BGA Rework Solutions

4.1.3.6.3 Conduction

Conductive tools heat by contact. Solder joints are heated quickly, whereas the substrate and adjacent components are barely warmed. The typical removal time for a power IGBT chip is less than 30 sec. Moreover, these tools are low cost and are quickly mastered by most operators to yield reliable and repeatable results. One drawback is the conduction technique cannot be used to readjust misaligned components.

The following is a list of possible suppliers for conduction rework station:

- Unite Equipment
- Micro Join

Note:

- Pb-free solder rework is more difficult than Pb solder because Pb-free alloys do not wet or wick as easily as the Sn-pb solder. The soldering parameters must be modified for higher melting point and poorer wet ability of the Pb-free solder. The “mixing” of Pb and Pb-free solders during repair/rework is a concern. Here, if a Pb solder joint is repaired with Pb-free solder, the reliability of the resulting joint is similar to that of the Pb joint. However, repairing a Pb-free joint with Pb solder would downgrade the reliability.
- The repair/rework station must be well ventilated or equipped with fume-extraction system to prevent any health hazard, such as asthma, caused by flux fumes.

4.1.4 Power Interconnections

The most common power interconnection method is wire bonding, using either gold or aluminum wires. In a power IGBT module, heavy aluminum wires are attached between the top aluminum metallization of the IGBT/FRED surface and the ceramic substrate by ultrasonic wedge bonding. This is a mature and reliable process. The equipment used can be highly automated with a sophisticated pattern-recognition system, such as the Autodyne 360. The bond quality can be improved further by installing a “smart” power generator, such as those offered by Verity.

Another interconnection method, pressure contacts or compression bonded encapsulation (CBE), is being used mostly in very high rectifier and SCR modules (such as Powerex's ED41 family). This method provides excellent thermal fatigue capability under high cyclic loads, but the electrical and thermal contacts are inferior. In this approach, each power chip is isolated separately from the copper base plate. The isolation used is usually BeO ceramic. The chip is sandwiched between top and bottom copper electrodes. The shape and size of the electrodes depend on the circuit configuration. Compression pressure is applied to the chips through a steel spring disc, which is placed on the top electrode and bolted to the baseplate by two to four mounting screws. Typical pressure applied is 500 lb/in². Because all contacts are made by pressure only, parallelism, flatness, and surface condition (such as cleanliness, burrs, cracks, etc.) are critical to achieve *uniform pressure*. In the case of SCR, the gate wire is usually attached separately by soldering.

In general, the production costs for this method are high, due to the high labor-intensive operations and the complicated mechanical structure needed to provide the mounting pressure. The latest IGBT chip, with its ultrathin NPT structure (~100 μm), will make this pressure contact approach a challenge. Semikron has offered a series of IGBT intelligent power modules, MiniSKiiP, using a combination of pressure-contact and DCB technologies. Both Westcode and Toshiba have introduced discrete IGBT devices in industry-standard compression-type capsules, with a current rating from 400 to 1000 A and voltage from 500 to 2500 V.

Key Bellevilles, Inc. is a possible supplier of spring discs.

4.1.4.1 Ultrasonic Wire Bonding

Compared with pressure contact, ultrasonic wire bonding is much simpler. It involves the use of aluminum wire, which is fed through and under a bonding wedge. During bonding, the wedge presses the wire against the metal termination pad, and ultrasonic energy (usually 20 to 60 kHz) is applied to the wedge. The wire is rubbed against the contact, causing local heating and a metallurgical weld. The thin oxide coating on the aluminum wire is ruptured, and the oxide tends to help the friction heating process, giving a very reliable bond. After the first bond has been made, the substrate is moved relative to the wedge, pulling the wire through the hole in the wedge. The substrate movement can be in one direction only: in the direction of the wire feed. The substrate is positioned until the wire is over the second termination pad, and the process is repeated. On completion of the second bond, the wire is clamped and tagged away from the bond, leaving a short tail. In the latest Orthodyne 360 model, the bond head can actually move in four directions: 6" in X and Y, 1" in Z, and 360 degrees in rotation. Bond angles can also be programmed to be independent of wire direction, making the bonding process a lot more flexible than the popular manual version Model 20.

Orthodyne is a possible supplier of ultrasonic aluminum-wire bonder.

The following list contains some useful information about ultrasonic aluminum-wire bonding:

- The first and second bonds are aligned in a straight line, parallel to the direction of the aluminum wire from the spool to the tool (Model 20).
- There are two settings each for the first and second bonds. These settings are time and power (or force).
- To start, adjust all four settings to about one quarter of their full values.
- Place a blank DCB-ceramic substrate on the bonding chuck and clamp it.
- Try to put both the first and the second bonds on the pad. If there is difficulty, adjust the settings until the bonds can be made. Test the pull strength. For Φ 350- μ m wire, the pull strength should be 2.5 N. When the wire breaks, it should break at the wire loop instead of at the bonds. If the bonds are lifted, the settings must be readjusted.
- For the first bond, use the lowest force setting possible and adjust the time setting until a good, solid bond can be made. This is because the first bond will be placed on the IGBT, and excessive force can damage the chip.
- After satisfactory bonds have been made on the blank substrate, use a substrate with IGBT and rectifiers already attached. Try wire bonding to the IGBT chip.
- If a wire can be attached and pass the pull-test, test electrically to make sure that there is no damage done to the chip. If the chip fails electrically, the settings, especially the force or power setting, must be reduced until good, solid bonds are made that give:
 - Good pull-test strength
 - Good electrical test:
 - $V_{DSS} > 1200$ V at $I_{DSS} = 4.5$ mA
 - $V_{DS(on)} < 4$ V at $I_D = 100$ mA and $V_{CS} = 12$ V
- Always put the first bond on the IGBT and FRED chip. Avoid direct bonding from chip to chip.
- The major failure mode of IGBT module is at wire bonding. There are three reasons for this:
 - Excessive bonding force — Excessive bonding force can damage the chip. This is true especially for *emitter bonding*. The design layout of IGBT chip has the emitter-bonding pad sitting on top of gate metal, separated by a layer of SiO_2 . Any excessive bonding force can break this oxide layer and short the gate emitter, producing a failure.

- Mechanical scratches — Again, the mechanical scratches at the emitter pad can produce shorts. These scratches are normally caused by parts that are not clamped properly, by accidental movement of the bonder handle during bonding, etc.
- ESD — The gate oxide is susceptible to ESD damage during wire bonding.
- Due to the sensitive nature of the IGBT chip, the first five production units must be visually, mechanically, and electrically inspected. If one or two fail, a failure analysis must be done and corrective actions taken immediately. Another five production units will be inspected until there is no failure. If the number of failures is three or more, stop production and notify the production supervisor for disposal.
- Pull strength of Al wire is shown in Table 4.11.
- The closer the clamp to the feed slot/hole, the better are tail control, looping control, and termination.
- Bond looping should be adjusted properly. If the loop lags too much, there can be a short circuit between adjacent wires. On the other hand, if the loop is too tight, any excessive stress can lead to wire breakage.
- Use bond tips made of tungsten carbide and osmium alloy.
- Wire-bonding operations should be performed in a controlled environment, such as a laminar hood or cleanbooth.
- Always make sure that the bonding machine, operator, and all tablemats are properly grounded before bonding.
- The bonding operator should wear special, static-free finger cots or gloves.
- At the beginning of each work shift, the bonding machine must be checked by QC. If the pull strength fails the required limit, notify the production supervisor for disposal. Do not start until the machine is performing normally.
- Periodically calibrate the ultrasonic bonder in terms of the bonding-tool vibration amplitude.
- Wire bond can be reworked by removing the bond jerkily with a fine point in a direction of about 20 degrees from the metallization surface.

TABLE 4.11

Minimum Pull Strength of Al Wire

A1 Wire (μm)	Pull Strength
Φ 25	> 3 gm
Φ 50	> 8 gm
> Φ 300	> 2.5 N

In the 200-A power module, 0.012" aluminum wire is preferred over 0.020" wire for the following reasons:

- **Lower ultrasonic energy** — The 0.012" wire requires lower sonic energy than does 0.020" wire for bonding.
- **Better current distribution** — For instance, a 200-A IGBT module requires 2×100 -A IGBT chips. Each 100-A IGBT chip requires 10×0.012 " wires or 4×0.020 " wires. The 0.012" wires can provide 10 bonds and 10 stitches or 20 contact points on the IGBT surface, whereas the 0.020" wire provides only 8 contact points.
- **Thermal stress due to TCE mismatch** — Stress on 0.012" wire is only about half that on 0.020" wire.

The 200-A power IGBT module requires about 70×0.012 " aluminum wires. Even though this is a mature process, this high number of wires will come at expense of:

- Reliability
- Circuit inductance and capacitance

An *all-solder approach*,^{*32} as shown in [Figure 4.3](#), should therefore be considered. In this case, the aluminum wires are replaced by:

- Solder bumps on the power chips' top surfaces³³
- A bent copper electrode that connects these solder bumps to the ceramic substrate.^{34,35}

It is conceivable that this approach could greatly simplify the manufacturing process. One single solder reflow with one single solder can accomplish the following:

- Attachment of IGBT/FRED chips to the ceramic substrate
- Attachment of chip electrodes to the ceramic substrate
- Attachment of power terminals to the ceramic substrate
- Attachment of the ceramic substrate to the metal baseplate

For the standard assembly of the 200-A IGBT module, these operations will require:

- Two or three separate solder reflows at two or three different temperature profiles
- Two or three solders with different melting temperatures
- One or two separate aluminum-wire bondings

* Patent pending.

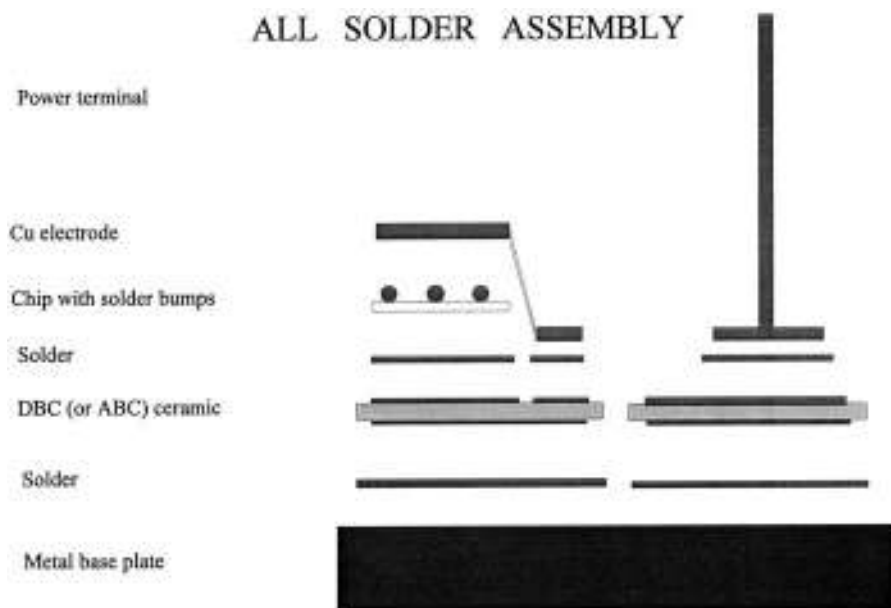


FIGURE 4.3

An all-solder assembly using power chips with solder bumps.

4.1.4.2 Solder Bump

The solder bump is literally a bump of solder material extended above the planar bonding metallization surface of the IGBT and FRED chips. The bump fabrication process is involved but mature.^{6,34} Basically, a pinhole-free passivation layer, such as Si_3N_4 , is deposited on the chip metallization surface at low temperature. The passivation is selectively removed to expose a good portion (to whatever design pattern) of the aluminum metallization bonding pad. An under-barrier metal (UBM), in this case copper, is then deposited over the exposed aluminum, followed by electroplating or screen-printing of solder. The UBM is adjusted to be about $45\text{ }\mu\text{m}$, which is the stand-off height after the solder bumps collapse. The total height of the solder bump ranges from 100 to $125\text{ }\mu\text{m}$, with a tolerance of $\pm 5\text{ }\mu\text{m}$. The size of the bumps depends on the design pattern.

None of the current IGBT and FRED manufacturers will supply chips with solder bumps. This solder-bumping process must be performed by an independent source, and most likely, it will be processed in wafer form. As for the solder, the same Pb-free material, such as Sn/Ag or Sn/Ag/Cu, can be used.³⁶ In this way, *the whole subassembly can be bonded together by one single solder with a very low elastic modulus, making the power module highly tolerant against thermally induced stress.*

The following is a list of possible sources that can provide solder-bumping services:

- Pac Tech
- Unitive Electronics, Inc.
- Focus Interconnect

The solder bumps must be inspected for:

- Coplanarity
- Shear strength
- Position accuracy
- Partial or defective bumps

Of these, coplanarity is the foremost problem, with defective bumps second in precedence.

The following are possible suppliers for solder-bump inspection:

- Dage Precision Industries
- Royce Instruments

Stencil printing and electroplating are two processes used to produce solder bumps.³⁷⁻³⁹ Stencil printing is becoming more popular because it offers a variety of time- and cost-saving benefits. This process is fast, because the solder paste is deposited across the entire surface of the IGBT and FRED wafers simultaneously. Fewer process steps are involved, there is no need for photomasking, and the productivity is high. Stencil printing also requires low capital investment. Even the most advanced printing systems are only a fraction of the cost of the conventional bumping thin-film system. The electroplating process is more involved and is more suitable for high-pin-count microprocessor products.

The key to the success of stencil printing is the proper design of the stencil. Issues that affect stencil-cutting technology for bumping include:

- Stencil thickness
- Aperture size
- Shape
- Orientation
- Position

For a bumping stencil, the cutting technology must be capable of producing multiple, closely spaced apertures to tight dimensional and positional tolerances. It is critical to maintain the accuracy of the aperture position as

close to the design as possible. Small excursions from the originally designed aperture size can lead to bump height variation, resulting in coplanarity failure.

Of the current technologies, only laser-cut and electroformed stencils can meet the requirements for printing effectively on wafers. Of the two, laser cutting is preferred because it offers aperture openings that have tapered walls with the opening size on one side of the stencil slightly larger than on the opposite side. As for stencil thickness, aperture size, and orientation, these all require experimentation to achieve the right combination for producing an acceptable transfer efficiency that satisfies past volume requirements while not crowding apertures too closely together. The preferred aperture shape is either circular or octagonal to reduce corner stress.

Milara is a possible supplier of stencil-printing systems for solder bump.

The flux used is water soluble or mildly rosin. It is best to use the finest solder powders in the stencil printing. For Pb/Sn solder, particle Type V distribution with 90% metal loading has been effective in bump printing. Defluxing after solder reflow with the electrodes connected to the bumps is critical because the surface must be clean enough for underfill.

Defluxing, in this case, is more involved because of the narrow gap. The requirements for the cleaning chemistry are:

- Good solvency for the flux
- Free-rinsing
- Low surface tension
- Low viscosity
- Environmental friendliness
- No or mild odor
- Low flammability

Several HFC and HFE solvents can satisfy these requirements.

Kyzen Corp. is a possible supplier of the defluxing solvent for the solder-bump process.

The reflow profile for the solder-bump process is very similar to that of normal reflow. The only probable change required is to extend the preheat zone so as to “freeze” the solder bumps to minimize slumping that may occur when the temperature reaches liquidus.²¹

For the 200-A IGBT module, there are eight electrodes required for the all-solder assembly: four for the IGBT and four for the FRED chips. These can be part of a stamped lead frame, which is formed to the desired configuration and eventually trimmed after the solder reflow. To carry 200 A, the copper frame should be about 0.020" thick. This raises a concern about the thermal mismatch between the copper and the power chips. However, the following five factors will help to alleviate this mismatch:

- **Bump height** — A thickness of 100 to 125 μm will contribute to a reduction in the stress on the chips by having a greater ability to flex when the force is applied.
- **Bump spacing** — For similar reasons, spacing between bumps distributed uniformly over the area of the chips will also reduce stress.
- **Bump material** — The use of compliant solder material, such as Sn/Ag or Sn/Ag/Cu with very low elastic modulus, will enable the bonds to absorb much of the thermal stress, thereby minimizing the effect on the power chips.
- **Bump size** — Solder bumps with large solder balls can generally provide good thermal-fatigue reliability. However, larger balls may show weakness in mechanical stress and may therefore require an underfill coating for strengthening.
- **Electrode material** — Besides Cu, Cu/Be alloy can be used as electrode. This will be much stronger mechanically and better thermally matched but at slightly higher cost. Alloy composition of 98 Cu/2 Be is commonly used.

4.1.4.3 Underfills/Topfills

This is a low-viscosity coating that is dispensed between the electrodes and the chips, filling the space between bumps. It has high wetting and penetration properties. Typically, the coating is epoxy based.

This underfill material performs several functions:^{40–42}

- Reduces and redistributes the stress and strains on the solder bumps by forming a strong adhesive bond
- Improves thermal conductance through the top surface
- Prevents the entry of contaminants

Requirements for this underfill coating are the following:

- Low elastic modulus
- Low viscosity
- High wetting
- High purity and freedom from ionic or corrosive constituents
- Fast cure (typically 5 min using variable frequency microwave [VFM])
- Spherical fillet particle less than half of the gap size
- Reworkability

Underfilling is not an established SMT process. Hence, proper material selection becomes one of the most essential parameters for reliability

performance and process ability. There are two methods to apply the underfill coating:

- Capillary (by dispensing)^{40,41,43–45}
- Glob (by printing, dispensing, or spin coating)^{40,43,44,46}

4.1.4.3.1 Capillary

This is the more common of the two methods. *The underfilling process is performed after all the solder reflow operations.* Here, the underfill coating is carefully dispensed into the 0.004 to 0.006" gap between the power chips and the top electrodes. The dispensing should be done along one edge only so as to prevent entrapped air. Capillary action pulls the underfill across the chip to fill the gap completely between the chip and the electrode. After the gap is filled, additional underfill may be dispensed along the sides of the chips to form a fillet. Filleting increases the thermocycle performance the chips, especially for larger chips.

Before dispensing, the underfill is heated to about 80°C to lower its viscosity. Heating also lowers the contact angle between the underfill and the substrate, creating strong capillary forces that pull the coating across the chip. In some equipment, the entire subassembly is heated to lower the viscosity further and improve the adhesion of the underfills. Wetting agents, such as silane compounds, may be added to improve wetting and also to allow underfill to flow up the sides of the chips to form a fillet, a process called *self-filleting*. The dispensing needle is typically 0.016 to 0.020" in inner diameter.

It is essential that there are no voids in the underfill. This will lead to early solder-joint failure. Precise control of the volume of underfill material and time allowed for capillary flow is necessary to achieve consistent results. In addition, because most underfills are epoxies that change viscosity over time during their usable pot life, the dispensing system should have a method of compensating for the volume of dispensed material, regardless of viscosity. *A positive-displacement piston-valve dispensing system* should therefore be used.

In general, the process windows for the flow temperatures, dispensing pattern, and time must be established for each individual application and material.

The following is a list of possible suppliers for the capillary type of underfills:

- Loctite Corp.
- Ablestik Electronics Materials & Adhesives
- Dexter Electronic Materials

4.1.4.3.2 Glob

This is a new method and requires a specially formulated underfill coating mixed with solder flux. Here, *the underfilling is performed before the solder reflow operation*. The underfill coating is dispensed as a glob on top of the power chips. The top electrode is then lowered into the coating with sufficient force to ensure contact between the electrode and the solder bumps. Typical placement force ranges from 150 to 350 g, depending on size and the bump counts. The whole subassembly is then reflowed to form solder interconnects. A secondary cure for 5 min in VFM or for 1 hour at 150°C in a conventional oven is needed after the reflow to create a stress-relief underfill layer.

The potential for this method is that the underfill can be applied on a whole-wafer basis. Solder-bumped wafers will be screen-printed or spin coated with underfill on the bumped side. These underfills will be dried to a solid, bondable film similar to wafer-level adhesives. The coated wafer will then be cut to form preunderfilled chips that can be handled like other components. The wafer-applied, reworkable underfill process promises to eliminate many costly off-line production steps currently limiting underfill technology, including the individual underfill of each chip and the separate curing step.

The following is a list of suppliers for the glob type of underfill:

- Emerson & Cuming
- Kester Solder

4.1.4.4 Solder Bump Pattern

Most available IGBT chips have multiple emitter bonding pads pattern, in which case the solder bumps can be fabricated on top of this pattern. Alternatively, a new custom pattern can be designed, which can be a square or rectangular matrix, depending on the size and shape of the power chips. For a square chip, the matrix can be one of the following:

- 4×4
- 5×5
- 6×6

The actual shape of the bump can be either circular or octagonal to reduce any corner stress.

4.1.5 Electrical and Thermal Testing

4.1.5.1 General

The power module is the power transmission component used in a 75-kW, three-phase constant voltage, constant frequency (CVCF) power supply

TABLE 4.12

Wire-Bonding Assembly vs. All-Solder Assembly

	Al Wire-Bonding Assembly	All-Solder Assembly
Reliability	Decreases as the number of aluminum wires increases	High
Current distribution	Depends on the number of wires	Uniform
Thermal performance	No effect	Two-sided cooling
Interconnection inductance	Wire inductance	Electrode inductance
Coplanarity	Not an issue	Needs to be inspected
Strength	Need to inspect aluminum wire pull strength	Need to inspect solder-bump shear strength
Manufacturing process	A 200 A IGBT module requires three solder reflows, two wire bondings	One single solder reflow for bonding — power chips, ceramic substrate, power terminals, metal heat sink
Cost	Low material cost High assembly cost	High material cost Low assembly cost

inverter. Each phase uses a half-bridge capable of transmitting 200 A and blocking 1200 V. The modules are sequenced at 8 kHz to generate a three-phase AC output. Because these power-generating systems are stand-alone units, ultrahigh reliability, competitive price, and superior performance through precision manufacturing and comprehensive testing must be achieved.

With reliability, price, and performance all being of paramount importance, we will adopt an approach to production testing that will utilize statistical analysis to optimize throughout and maintain near-perfect yield. A complete component and power module test history will be maintained for every power module to enable accurate product analysis. Each IGBT module shall have bar-code identification and a file with a history of material characteristics, process parameters, component test results, and module test results. Because these modules are difficult to repair, any failed module will be returned to the failure analysis laboratory to determine possible causes. The knowledge gathered from the test history, along with the results of the failure analysis, will be used for product improvement.

Figure 4.4 shows the basic power section of the module. The test equipment chosen for engineering and production testing must be effective for these basic functions. It must also have the flexibility to increase capability as more-complex features are added.

There are four phases of testing to be considered:

- Engineering evaluation
- Incoming inspection
- In-process production testing
- Final testing of finished modules

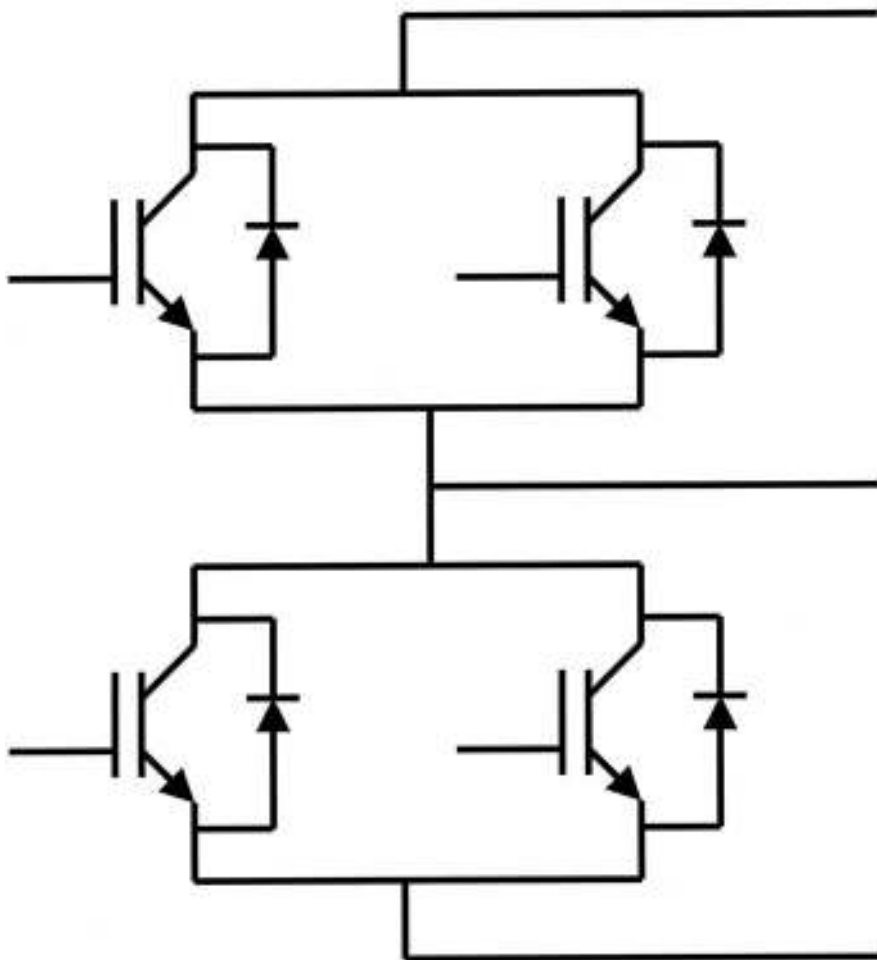


FIGURE 4.4
Half-bridge configuration of paralleled IGBT.

For engineering evaluation and preproduction testing, the equipment needed is a PC with a general-purpose interface bus, a Tektronix Model 371A curve tracer, an Analysis Tech Phase 10 thermal analyzer, and a high-current/high-voltage power supply to simulate short-circuit test conditions. The curve tracer can provide a family of curves accurately describing the on (200 A) and off (1200 V) characteristics of each IGBT and FRED in the module. The thermal analyzer will provide thermal impedance curves showing the heating characterization, enabling insight into the thermal performance of each power component in the module. The information obtained with this equipment, along with the test data supplied by the chip manufacturer, should provide sufficient knowledge to characterize completely each module assembled during the development and preproduction phase.

Incoming electrical components, along with their supporting data, will be logged in as outlined in Chart 4.1. Generally, semiconductor manufacturers supply test data with the material. These data will be entered into the product

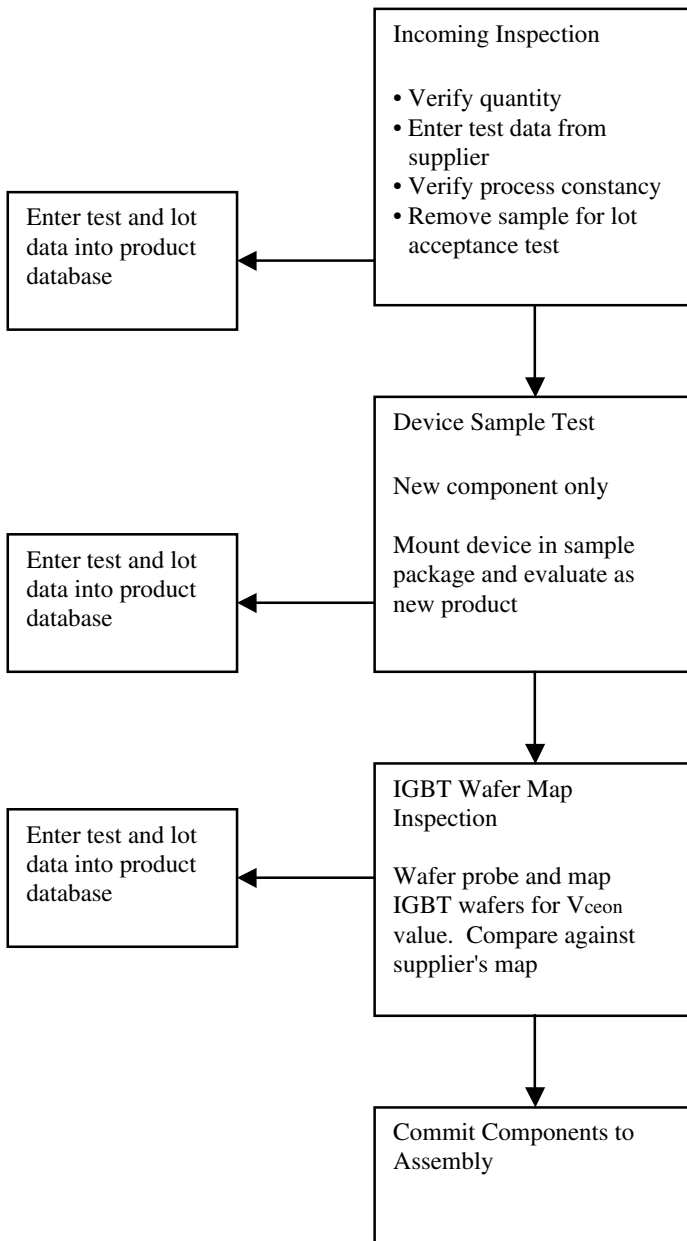


CHART 4.1

Component incoming acceptance flow chart.

database. The data will include probe results on static parameters, such as leakage current, breakdown voltage, threshold voltage, V_{CEON} , and V_{ECSAT} for the IGBTs and breakdown voltage, t_{tr} , and V_{FM} for the FREDs. Usually, specific and statistical data are available for each wafer in each lot. As the module becomes more complex, additional data taken from more complex integrated circuits will be required.

During production, the subassembled IGBT modules are subjected to in-process testing. Typical parameters that are tested are I_{CES} , V_{CES} , I_{GES} , V_{GES} , V_{CESAT} , and V_{GETH} . Here, a semiautomatic probe station can be used to perform the task.

The finished modules will undergo a battery of tests as described in Chart 4.2. As historical data are collected, the necessity for each test will be reviewed, and tests will be sampled or eliminated to reduce manufacturing costs.

Static and dynamic testing will be done before and after the high-stress short circuit and safe operating area tests in order to find out whether these tests are causing any degradation. One hundred percent thermal testing will be performed to evaluate the integrity of the die and wire bonds and the thermal impedance of the module.

Records of all final test data will be displayed in bar code or 2D data matrix symbol for each module. (See Appendix B.)

Note: All testing should be performed in an ESD-protective environment. See [Section 4.3](#) on ESD precautions when handling the finished IGBT module.

4.1.5.2 Incoming Inspection

Each component used in the assembly of the module will be tested and the test data recorded. IGBT and FRED components are common to all modules and will be treated as follows. The inspection of other components, as they are designed into the module, will be addressed as they are selected. See [Table 4.16](#) for incoming inspection.

4.1.5.2.1 IGBT

Random samples are selected from the IGBT lot and tested on the curve tracer to electrical specification. [Section 4.2](#) discusses inspection to other specifications. The sampling plan should be at a level of AQL 0.65 or better. For V_{CESAT} , special attention should be given to the wafer mapping. MOSFETs share current when used in parallel; IGBTs tend to hog current when in a parallel configuration. This is due to the negative effect of temperature on collector to emitter saturation voltage, V_{CESAT} . The current hogging by one IGBT may cause it to overheat and self-destruct. To minimize current hogging, IGBTs, when used in parallel, will be matched in collector-emitter saturation voltage, V_{CESAT} . They must also be thermally coupled in the final module to ensure collector-to-emitter voltage tracking.

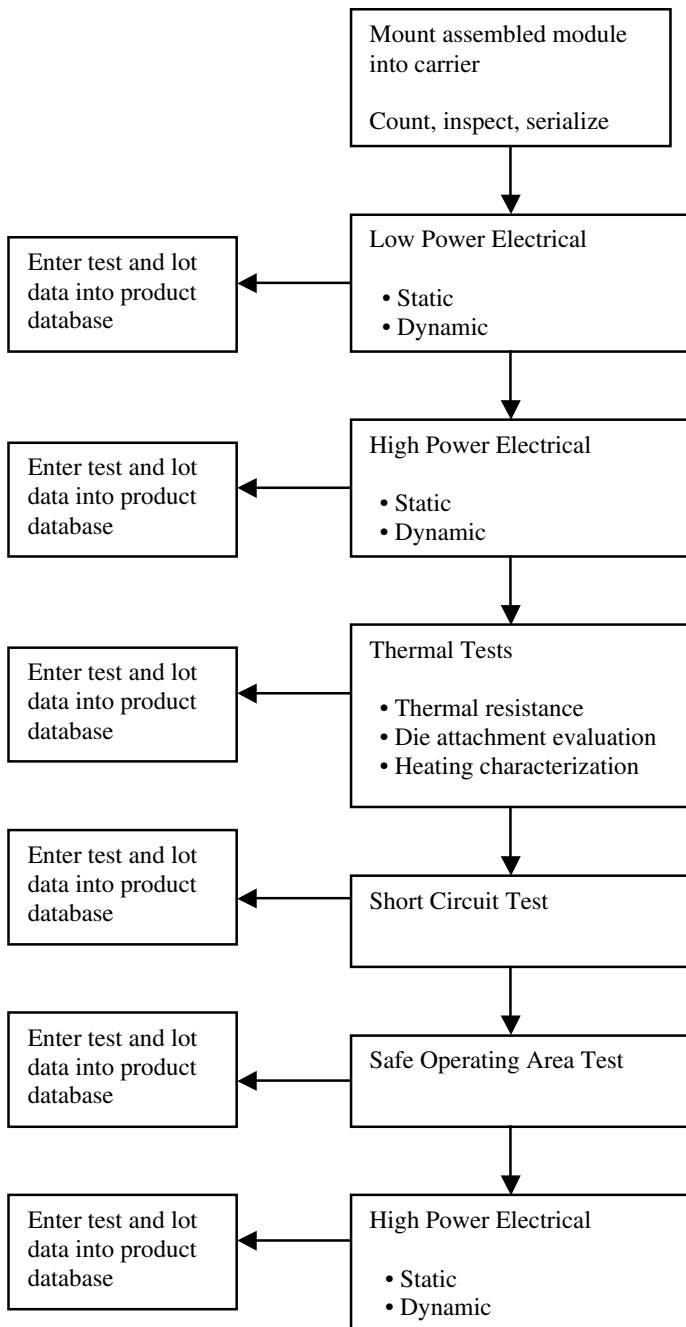


CHART 4.2

Electrical and thermal test sequence.

Each IGBT wafer is to be probed and mapped for V_{CESAT} . This may be done by the user or the IGBT manufacturer. Because the IGBT manufacturer probes these dies to determine their specifications, it appears that mapping and data logging are best accomplished by the IGBT manufacturer. Dies with V_{CESAT} within 0.30 V of each other may be used together. Tests for V_{CESAT} are performed using an automatic component tester capable of data logging and an automatic wafer probe with a Kelvin probe configuration. During assembly, computer programs will use the logged data to select the IGBTs that are to be used in parallel in each module. This method will ensure near-perfect matching and maximum utilization of IGBT chips. The accuracy of this wafer map is therefore critical and must be closely inspected. If the user is doing the wafer mapping, data logging may be accomplished under the control of an IBM PC, connected to the tester and wafer probe. Software is available through many test equipment manufacturers, such as LabView software from National Instruments or wafer-map software from Kinesys Software. The result of this in-house mapping must also be carefully inspected.

Programmable testers are available for IGBT probe testing from Tektronix, Lorlin Test Systems, Tesec Inc., FET/Test, Scientific Test, Hasper Technologies, and ipTest Ltd. Because automatic test equipment is necessary for electrical testing of the completed module, the same test equipment can be used for wafer probing. Some of the currently available test equipment is discussed in the electrical tests section that follows.

Automatic wafer-probing equipment is available from Electroglas, Pacific Western, and Wentworth for \$50,000 to \$100,000. A single wafer probe and a trained operator will be adequate for a reasonable volume of IGBT dies. The wafer probe manufacturers mentioned supply a wide variety of probing equipment, from semiautomatic to high-volume, fully automatic with optical recognition.

Because IGBT wafers are very thin and are limited in size to 5" or 6" in diameter, an Electroglas model 2000 series automatic wafer probe with 6" wafer-size capability will be satisfactory. The 2000 series has automatic wafer loading, eliminating the risk of damage in hand loading. Wafer loading uses the same cassette used for wafer shipping. Wafer alignment is automatic. The model 2000 probe also has mapping and data collection networking connectivity to facilitate IGBT sorting. The series 2000 requires input power, air, and vacuum (3 A, 75 psi at 2.3 scfm, 23 in Hg at 3 scfm); it requires a 4-ft² floor area.

It should be noted that more recently, non-punch-through IGBTs (NPTIGBT) have been designed to have positive V_{CESAT} of 1.12 to 1.29 V at $I_c = 10$ A. This may enable parallel operation of the IGBTs without the need for precision matching.

4.1.5.2.2 FRED

Fast recovery epitaxial diode (FRED) chips will be tested to specification by the semiconductor manufacturer. Test data may be verified by mounting a

small sample of FRED chips and testing for t_{rr} . Static parameters can be tested on a curve tracer.

4.1.5.3 *In-Process Production Testing*

As shown in by the manufacturing flow charts in [Section 4.4](#), after each high temperature over reflow and wire-bonding operations, the IGBT subassembled modules are tested to detect any possible degradation caused by the following:

- Mechanical damage
- ESD
- Contamination

The key IGBT parameters tested to the rated specifications at 25°C are:

- I_{CES}
- V_{CES}
- I_{GES}
- V_{GES}
- V_{CESAT}
- V_{GETH}

A manual or semiautomatic probe station can be used for this purpose.

These tests will ensure that all subassemblies at different stages are fully tested and inspected before committing to further assembly.

4.1.5.4 *Final Testing for the Finished Module*

After assembly, power modules are subjected to electrical and thermal testing. The module lot should be *serialized* because all testing data of individual modules are recorded. These data will be displayed as part of a barcode or 2D data matrix symbol to be attached to the module. (See Appendix B.)

4.1.5.4.1 *Electrical Tests*

Electrical tests include static (DC test), dynamic (AC switching test), short circuit, and safe operating area (SOA). Because there is access to the collector, emitter, and collector/emitter terminals of the power module, the characteristics of each IGBT parallel pair and of each FRED parallel pair can be tested individually. The IGBT pairs and FRED pairs may be examined separately for their electrical and thermal impedance characteristics. As the module increases in complexity, tests can be added to test the additional circuitry.

The initial test will be a low-power static test to verify that the components have not been damaged during assembly and that the electrical interconnects

are as designed. Usually, measurement times are significantly longer than the small time constants of the devices under testing, which means steady-state operation is characterized. Failures of the static electrical test are recorded and the results immediately sent to assembly for corrective action. Static tests may be used to verify test results that were reported by the component (chip) manufacturer. Discrepancies will be reported to the supplier.

Following the static tests are switching tests to determine and record the speed of each power component and of the components as a unit. Of particular interest is the inductance introduced by the relative positions of the components. Because assembly should not have changed the dynamic characteristics of the components, the dynamic testing of the power module in its initial version should indicate the dynamic qualities of the components. These test results can be used to predict the dynamic switching losses of the module in its application. As the module becomes more complex, dynamic testing will become more significant.

After static and dynamic testing at low power, the module will be subjected to high-power testing to verify the integrity of the thermal structure. After these tests, short-circuit and SOA tests, combined with thermal analysis testing, will be used to ensure the quality and reliability of each module.

4.1.5.4.1.1 Static and Dynamic Electrical Tests — Electrical tests include static and dynamic testing at two temperatures. These tests will include those shown in [Table 4.13](#).

Tests that result in power being dissipated will be done in a pulse mode so as not to heat the device under testing (DUT). Initially, 100% of finished modules will be tested at high power with heat sink. After enough data are accumulated to ensure test correlation, tests will be in a low-power pulse mode with a sample power tested.

4.1.5.4.2 Short-Circuit Tests¹⁻³

Short-circuit tests shall be carried out through the use of power supply capable of delivering 600 A at 1200 V. The power supply shall be adjusted so that the voltage spike at turn-off, due to stray inductance, does not exceed the voltage rating of the IGBT. The length of the power test leads must be kept to a minimum to minimize the voltage spike at turn-off. The unit under testing will be attached to a heat sink similar to that used in the final application. With power applied to the collector of the upper IGBT and the emitter of the lower IGBT, and with the upper IGBT biased on, the lower IGBT will be pulsed on for 10 μ sec. This condition will be repeated 10 times at 0.1-sec intervals. The unit under testing will be returned to electrical and thermal resistance test to be inspected for performance degradation. Initially, short-circuit testing may be carried out on all units. After correlation between thermal resistance, electrical, and short-circuit tests has been established, the short-circuit testing shall be carried out on a sample basis.

TABLE 4.13

Static and Dynamic Testing Parameters

Symbol	Parameter	Definition
<i>Static</i>		
I_{CES}	Collector-emitter leakage Current	I_C @ $V_{CE} = V_{CES}$, $V_{GE} = 0$, gate-emitter shorted
I_{GES}	Gate-emitter leakage current	I_G @ $V_{GES} = V_{GES}$, $V_{CE} = 0$, collector-emitter shorted
V_{GESAT}	Gate-emitter threshold voltage	V_{GE} @ $I_C =$ specified mA, $V_{CE} = 10$ V
V_{CESAT}	Collector-emitter saturation voltage	V_{CE} @ $I_C =$ rated I_C and $V_{GE} = 15$ V
Q_G	Total gate charge	Charge on gate @ $V_{CC} - 0.5 \sim 0.6$ $V_{CS} = I_C =$ rated I_C , $V_{GE} = 15$ V
V_{FM}	Diode forward voltage	Diode voltage @ $I_C =$ rated I_C , $V_{GS} = 0$ V
<i>Dynamic</i>		
C_{ies}	Input capacitance	Gate-emitter capacitance with collector shorted to emitter
C_{oes}	Output capacitance	Collector-emitter capacitance with the gate shorted to the emitter
C_{res}	Reverse transfer capacitance	Gate-collector capacitance with the emitter connected to the guard terminal of the impedance generator
$I_{td(on)}$	Turn-on delay time	Time from $V_{GE} = 0$ V to $I_C = 10\%$ of final value
t_r	Rise time	Time from $I_C = 10\%$ of initial value to $I_C = 90\%$ of final value
$I_{d(off)}$	Turn-off delay time	Time from $V_{GE} = 90\%$ of initial value to $I_C = 90\%$ of initial value
t_f	Fall time	Time from $I_C = 90\%$ of initial value to $I_C = 10\%$ of initial value
t_{rr}	Diode reverse recovery time	Time from $I_C = 0$ A to projection of zero I_C from I_{rr} and $0.5 I_{rr}$ points with $I_C =$ rated I_C and at specified di/dt
Q_{rr}	Diode reverse recovery charge	Area under I_{rr} curve from $I_C = 0$ A to projection of zero I_C from I_{rr} points and $0.5 \times I_{rr}$ points with $I_C =$ rated I_C and at specified di/dt

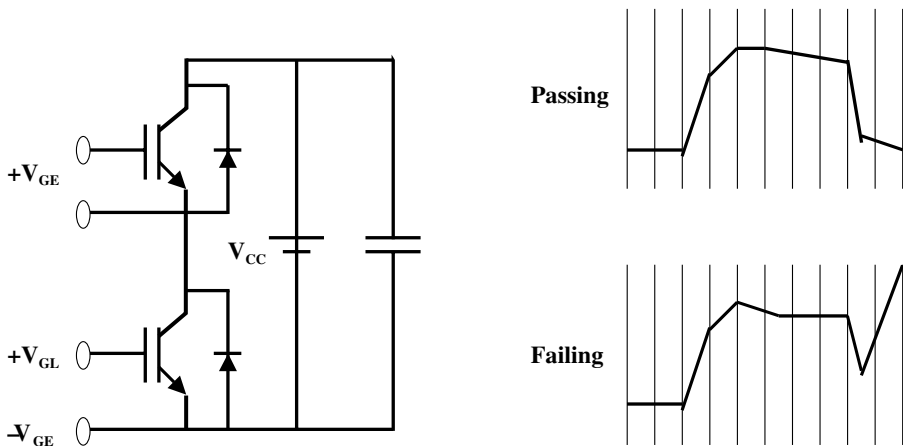


FIGURE 4.5
Short-circuit testing.

The circuit shown in Figure 4.5 can be used for the short-circuit testing.

4.1.5.4.3 SOA Test¹⁻³

Because of their internal structure, IGBTs can encounter thyristor latch-up during turn-off with an inductive load. This latch-up means loss of gate control and eventual destruction of the device. The SOA test is designed to identify any IGBT components that tend to demonstrate thyristor latch-up. Initially, SOA testing may be carried out on all units. After correlation among thermal resistance, electrical, and SOA tests has been established, the SOA testing shall be carried out on a sample basis.

The test circuits shown in Figure 4.6 simulate the conditions that could lead to the latch-up condition.

Because of the high current and low stray inductance requirements for the short-circuit test and for the SOA tests, the tester configuration for each of the devices to be tested should be tailored specifically to the application.

4.1.5.5 Test System Considerations

Many issues must be considered when choosing a test system. Design and development engineering needs accurate equipment for design characterization. The equipment must be fast and accurate for production and able to assemble test data for statistical analysis. Very importantly, the test system chosen must be able to keep up with new product features as they evolve. The test system must be able to withstand the conditions presented when testing a shorted or otherwise defective device, without damage to the system. This is particularly difficult when testing power devices such as IPMs.

A system with open-frame architecture will enable testing of present features while having the flexibility to adapt to future test requirements.

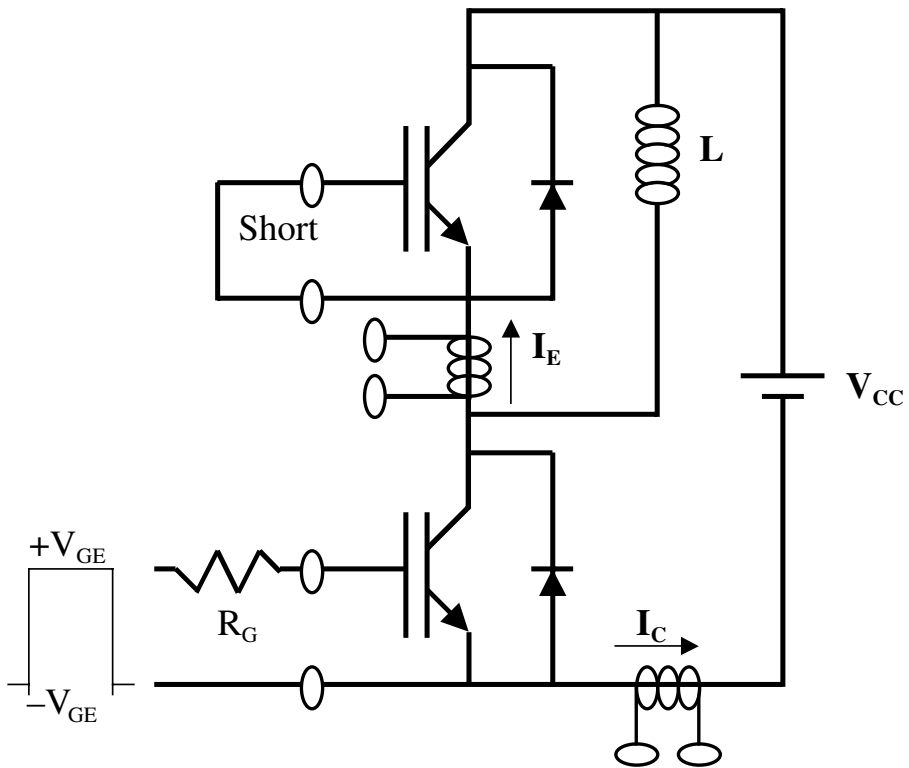


FIGURE 4.6
SOA test circuit.

Testers are commercially available that perform most of the tests mentioned above. Programmable testers are available from:

- Lorlin Test Systems, Natick, MA
- Tesec, Inc., Japan
- Tektronix, Inc., Beaverton, OR
- ipTest, United Kingdom
- Scientific Test, Inc., Garland, TX
- FET/Test, Morgan Hill, CA
- Agilent Technologies, Palo Alto, CA

Tektronix's 371A digital storage curve tracer appears to have the most versatility to perform wafer-probe tests and for characterization of finished modules. The Tektronix 371A is a programmable curve tracer capable of sourcing up to 3000 V and 400 A. At peak power, it can source 20 A at 2000 V. The high-voltage collector mode permits testing the off-characteristics of the IGBT chip or of the power module up to 3000 V. The pulsed high-current collector mode provides output current pulses greater than 400 A peak for

testing on-characteristics. In the sweep measurement mode, it automatically constructs a family of curves while stimulating the device with low-duty cycle pulses, without excessive heating of the device. The Tektronix 371A costs less than \$50,000, including cables and National Instruments' LabView driver. The limitation here is the Tektronix 371A cannot perform high-voltage/high-current testing. The 371A should be considered for electrical testing and device characterization during the initial phase of IPM product development.

For production testing, a Lorlin Test Systems LEM IGBT tester may be used. The Lorlin LEM test system may be configured to test the basic power module, and it is upgradeable to meet the needs of more complex IPMs. The LEM IGBT tester has the ability to measure switching characteristics on half-bridge modules and on IGBTs and MOSFETs.

In the half-bridge configuration, the system may be set to simulate the module's intended application. Current may be set to flow through the inductive load and the module under testing. Switch settings make it possible to measure one of the IGBT chips together with the free-wheeling diode of the other leg of the half-bridge as the module is in its application.

The system is fitted with static and switching measurements on both resistive and inductive loads, including gate characteristics. This system includes a digital oscilloscope, which enables switching energy measurements. Accuracy is within 5% for high-power devices. This test set also allows characterization measurements of short-circuit withstand at 2.5 times the rated current and gate capacitance characteristics.

Lorlin LEM is modular in design, enabling choice of voltage and current. Available are 250 or 2500 A in current and 100, 1000, or 5000 V in voltage.

A typical Lorlin test system to test IGBT or MOSFET power modules consists of the following:

- **Transistormeter TRds 0215-1020** — For measurement of static and dynamic measurement on IGBT devices: 250 A and 1500 V on inductive load, and 1000 A and 2000 V for static parameters. This unit contains the power supply, power generators, inductive load, double gate drive (± 1 to 30 V, 50 nsec t_r/t_f , 0.5), digital oscilloscope, voltage and current measuring systems, and protected output for the module under testing.
- **The control unit** — Consisting of an industrial PC with Ethernet board, modem, GPIB bus, LCD screen, floppy disk drive, and keyboard with trackball.
- **A connecting system** — Connections to IGBT modules for dynamic testing require short, low-inductance connections. The system includes a thermostatically heated base plate, room temperature to 200°C, and a board of nail-type adapters. The communication from IGBT to IGBT of the same module is controlled by the tester and made by means of low-inductance commutation devices. Each IGBT

module requires a specific adapter, which, along with the gate resistor, can be changed.

Dynamic measurements on the transistor include t_{sv} , t_{si} , t_{rv} , E_{off} , $t_d(on)$, t_r , di/dt , I_{peak} , and E_{on} . Dynamic measurements on the free-wheeling diode include I_{rr} , t_{rr} , Q_{rr} , and E_{rec} . Static measurements include I_{GES} , Q_G , $V_{GE(th)}$, and V_{FM} (diode).

The proposed Laurin test system costs \$275,000.

Tesec Corporation also configures a test system that may be used to test the IPMs. Tesec uses an open-frame architecture that is under control of a PC. Their test system will have four integral parts: Mainframe tester, test station A, external tester (9424-KT/B), and external tester (3430-SW).

4.1.5.5.1 Mainframe Tester

This is a model 881-TT/A tester with access for programmable data collection, up/download, and printing. It operates under Windows 98 and can be multiplexed for up to five test heads. See [Table 4.14](#).

4.1.5.5.2 Test Station A

This station will interface with a die probe if necessary. It includes a high-current adapter (200 A) with a 32-pin programmable scanner enabling IPM testing. It will allow full DC parametric testing of up to 32 pins (1200 V/200 A).

4.1.5.5.3 External Tester (9424-KT/B)

This external tester enables testing of thermal resistance and thermal impedance. This could interface with test station A, enabling one pass DC parametric testing. The programming is the same program as for the DC testing. [Table 4.15](#) presents more detail specifications of the tester.

4.1.5.5.4 External Tester (3300-SW)

This external tester enables dynamic testing of t_{on} , t_{off} , t_r , E_{on} , E_{off} , I_{cc} , t_{rr} , I_{rr} , Q_{rr} , SC , and UIS . MOSFETs and IGBTs can be tested. With this external tester, module testing is not possible at this time via programmable scanning.

Specifications for this specific application will be developed.

The cost for the Tesec system as described previously is approximately \$600,000.

4.1.5.6 Thermal Tests

Elevated junction operating temperatures in semiconductor devices can lead to premature aging and failure. The purpose of thermal testing is to evaluate the integrity of the thermal path between the IGBT and FRED junctions and the heat sink. Thermal testing is necessary for adequate production monitoring of component attachments and for the continued evaluation of newer

TABLE 4.14

881-TT/A Specifications

Host CPU	Personal computer
Operating system	Windows 98
Control CPU	68,000
Data display	4-digit high-speed A/D
Multiplexer	5
Voltage	1000 V (3000 V optional)
Current	20 A (200 A optional)
Test plan	250 tests max
Sort plan	250 sorts max

TABLE 4.15

9424-KT Specifications

Test programming	External PC
Memory	16 test programs
Forcing voltage	1~200 V
Forcing current (I_E/I_{DS})	0.01~50 A, 0.01~100 A (ΔV_F)
Sensing current I_M	1~100 mA, 1~400 mA (ΔV_F , ΔV_{CE})
Power forcing time	300 μ s~9.99 sec
Delay time	10~999 μ s
Upper limit/lower limit	0~999.9 mV/O~9999 mV
Measurement range	ΔV_{CE} : 0~9999 mV
Test result display	ΔV_{CE} : 0~9999 mV, ΔV_{CE} : 0~9999 mV
Judgment display	Pass, Low, High, Aval, Error, Osc, Open, Short, Conf
Binning	4 bin modes: Pass, Low, High, Reject

assembly techniques. The discussion of thermal testing includes temperature-sensing principles, sense junction calibration, thermal resistance, solder attachment evaluation, and heating characterization.

4.1.5.6.1 Temperature-Sensing Basics

Semiconductor p/n junctions possess useful characteristics that can be used for the measurement of junction temperatures. These characteristics are called temperature-sensitive parameters (TSPs). It can be shown that, under constant current conditions, the voltage drop of a forward-biased diode junction decreases linearly with temperature about -1 to -3 mV/ $^{\circ}$ C. This feature is the basis of temperature-sensing applications. The free-wheeling diode is part of the IGBT, and its forward-biased junction can be used to measure the junction temperature of the IGBT chip.

4.1.5.6.2 Sense Junction Calibration

IGBT calibration is performed with the baseplate at a stable temperature and with only the sense current for the free-wheeling diode, the TSP, applied.

Because the sense current is usually too small to cause any significant junction heating, the base-plate temperature will nearly equal the IGBT junction temperature. By collecting data over a range of base-plate temperatures, the diode junction voltages and the corresponding junction temperatures can be plotted into a best-fit straight line.

4.1.5.6.3 Thermal Resistance

To measure steady-state thermal resistance, the measurement of a device junction temperature during the application of continuous heating power is required. Thermal resistance, junction to reference in $^{\circ}\text{C}/\text{W}$ is defined as the difference between junction temperature ($^{\circ}\text{C}$) and reference temperature ($^{\circ}\text{C}$) divided by power dissipation (in watts) after the device has reached steady-state thermal equilibrium. To evaluate the power module, the reference temperature is the temperature of the base plate. The junction temperature is measured during brief intervals when the otherwise-continuous heating power is interrupted and the sense current is applied to the sense junction. The entire cycle — interrupting the heating power, applying the sense current, measuring the sense voltage, and restoring the heating power — occurs over tenths of a millisecond.

4.1.5.6.4 Solder Attachment Evaluation and Heating Characterization

In a transient condition, thermal mass must be taken into account. In the case of an IGBT stack, the heat initiates at the power chips, then progressively flows through solder 1, the ceramic substrate, solder 2, and the metal base-plate as a function of time. The heating step-response curve will therefore reveal useful insight into the cross-sectional view of the thermal resistance within the stack structure. For instance, for a short pulse of controlled duration, most or all of the heating can be limited only to the chip solder attachment layer. The measured result will be dominated by the thermal resistance of the chip attachment and can therefore be used to evaluate its quality. By comparing with the results from a known good chip attachment, this test can serve as a quick production screening for detecting low-quality die bonds. Likewise, longer heating duration pulses can be used to check other interface layers. [Figure 4.7](#) shows the typical heating step-response curve of a multilayer structure. The plateaus here represent the heating to thermal equilibrium of different layers. See [Chapter 5](#) for testing results.

4.1.5.7 Test Fixtures

Initially, the fixtures for testing will be of the laboratory type, using power supplies, a digital oscilloscope, and a thermal tester. Power connections will be of the short bus bar type, with connections to the module under test manually bolted to the bus bars. Signal connections will be manually attached. During the production phase, this set-up will be enhanced and used for new product development.

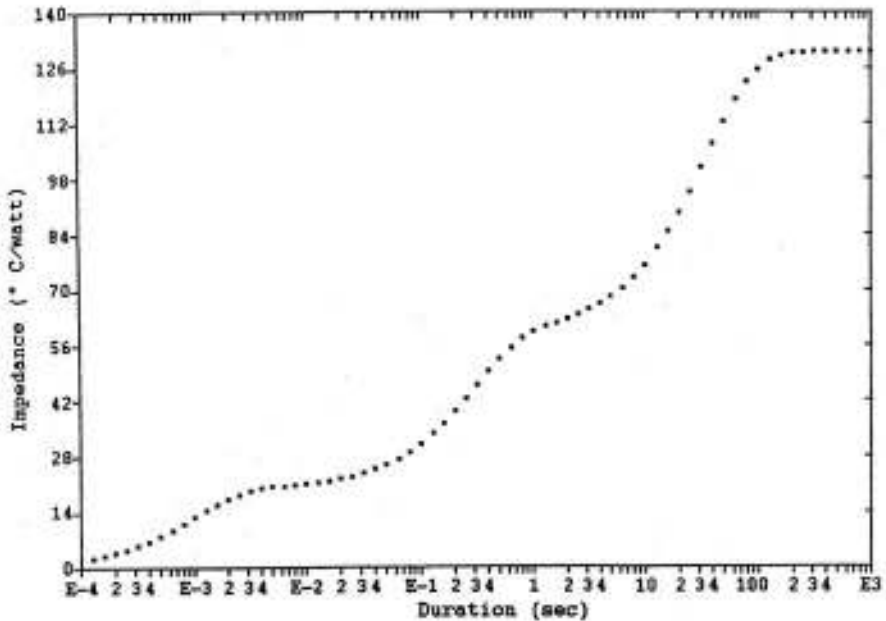


FIGURE 4.7
Example of log-time heating characterization.

In production, to facilitate all the tests required to ensure reliable performance of the module, a carrier will be designed that enables rapid and automatic insertion of the module into each test station. A carrier approach is recommended to obtain maximum repeatability and test flexibility. As the module evolves, necessary tests may be added without disturbing the critical inductance between the power test stations and the DUT. Also, test sequences may easily be altered when necessary. The carrier is to have three main power terminals and a bank of low-level signal connectors. The carrier will also have space for optical coupling for future applications. The module under testing will be bolted to the carrier via the three power terminals.

The carrier will be designed for automatic handling. The carrier and test head shall be designed so that the module will plug into the test head(s) of the various test stations. A mechanical forcing element will act as the heat sink for the module under testing. The forcing element shall also contain a heating/cooling device and a thermal couple, thus enabling temperature testing while providing accurate temperature monitoring of the module.

The testers that will be used are supplied with power cables suitable for the required test currents.

An alternative approach to using a carrier for automatic device handling is to test before bending the main terminals. With this approach, the main terminals act as the plug and the base of the module as the carrier. The test

head will be designed to accept the main terminals as well as the signal terminals.

Although this approach appears efficient for the module in its simplest form, the test head design limits the variety of module designs that can be tested. Also, after the power leads are bent into their final form, a low-power test should be performed to ensure that the bending has caused no damage.

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4.2 Process Control/Long-Term Reliability

4.2.1 Process Control

Process controls are inspection sites that are positioned strategically along the production line to monitor the process;^{1,2} these controls have already been established during the engineering phase. The flow charts in [Section 4.4](#) show the possible sites for these inspections. Mil- Std. 883, 105, J-STD-001, and IPC-A-610 Class 2 should be reviewed when setting up monitoring programs. Because the monitoring is performed on a sample basis, the results are basically statistical data that will provide a dynamic feedback during manufacture. These data should be real time and displayed. Any anomalies

will result in failure analysis, rework, or even process adjustment. The aim is to establish a *zero defect production line* that combines *in-process inspection using advanced tools* and *statistical process control* in a closed-loop environment.

4.2.2 Tools

Tests and measurements are essential in collecting these data, which must be accurate and broad ranged. This requires intensive use of the state-of-the-art technology. Newer and more powerful tools should be continually introduced to replace or complement the traditional, such as the high-power visual, 2D x-ray inspection, etc. Examples of the latest tools include the following:

- X-ray with 3D capabilities,^{3,4} or laminography
- Scanning acoustic microscope (SAM)⁵
- Optical profiling — Visual or far infrared
- Thermoacoustic imaging — Combination of infrared and acoustic technologies
- Deep view laser scanning microscopy

These tools are adequate to provide macroscopic information that will lead to an improvement of production yield. However, microscopic information, such as the microstructure of the solder joints, is also desirable. The formation of excessive intermetallic compounds can promote crack initiation and propagation, reduce solder joint strength, and be detrimental to the long-term reliability of the solder joints. Sophisticated analytical tools, such as 3D x-ray, SEM, etc., are therefore required to provide early information about long-term reliability without any extended life tests.

Two other tools of interest are thermal electrical mapping and thermal mechanical characterization. Thermal electrical mapping, or the distribution of junction temperature T_j of the IGBT chips, identifies the “hot spots” that can be destructive during a short-circuit operating condition. Infrared and liquid crystal thermography are the two most common techniques in thermal mapping.⁶ The thermal test dies method is also gaining importance but is most often used in the initial characterization of the product. The scanning thermal microscope and the laser thermoreflectometer methods are mostly restricted to advanced laboratory measurements. Thermal–mechanical characterization will provide useful information on the warpage and thermal stress distribution that has impact on long-term reliability.

4.2.2.1 Thermal–Electrical Mapping or IR Thermography

Thermal–electrical mapping, or IR thermography, is a kind of nondestructive in-line testing intended to improve production yield. IR mapping is based

on infrared imaging technology, which enables a quick and easy examination of electronic assemblies *before encapsulation*. When power is applied to the module, it heats in a characteristic manner, which is referred to as its *thermal signature*. This signature is captured using a digital IR camera.* Any defects, such as voids, cracks, opens, etc., will change the signature from its known good signature. The defective modules can then be repaired and reworked, without being scrapped. Liquid crystal thermography is also effective but is destructive. It involves painting the surface (chip, ceramic substrate, base plate, terminals) with a thin film of liquid crystal. When the module is powered, the liquid crystal will respond to an increase in temperature by changing its color.

4.2.2.2 Thermal–Mechanical Characterization

Thermal–mechanical characterization is a nondestructive measure of how reliably a module can function under temperature excursions. It provides useful information without actually performing extensive life tests. Mismatched CTE (coefficient of thermal expansion) values of package materials, such as IGBT chip/solder/ceramic substrate, ceramic substrate/solder/base metal plate, can cause significant deformation and stresses during high-temperature manufacturing processes. This thermally induced deformation or warpage can potentially lead to mechanical damages, manifested as cracks, fractures, or delamination. Some of these damages may appear during or after processing; others may be latent and surface during operation. Under these circumstances, the reliability of the module is severely compromised.

A characterization of the magnitude and distribution of the deformation or warpage at different temperatures will therefore provide practical information on how reliably a module can function under temperature excursions. By measuring the magnitude, the location, and the type of curvature of the warpage, *one can identify with high probability the areas where damage may occur*.

The deformation distribution can be obtained nondestructively by:

- Measuring and plotting the displacement at different points, using a profilometer
- Using optical profiling means, such as:
 - Noncontact optical shadow moiré interferometry⁷
 - Far infrared interferometry⁸

The acceptable displacement limits should be established through a series of initial correlation tests.

* In 2003, NIST has developed a high-speed IR thermography technique.

4.2.3 In-Process Inspection

There are three levels of in-process inspections:

- **Incoming inspection** — To inspect all incoming materials to the requirements of the specifications (in some companies, this is part of the vendor inspections performed at vendor locations)
- **Near-term (current)** — To monitor manufacturing process, to identify rejects, to act as a control mechanism on in-process yield loss
- **Long-term (time-dependent)** — To monitor parameters that have long-term implications to ensure long-term reliability

Note: The accuracy of any inspection and testing system should be at least three times better than the tolerance for the variable being measured. All inspection and testing systems must be periodically calibrated against standards whose calibration is traceable to National Institute of Standards and Technology (NIST) via primary standards.

4.2.3.1 A Partial List of Visual Inspection Criteria for IGBT and FRED Chips

- **Sampling level** — AQL-level: 0.65, level I, normal inspection
- **Rejection criteria:**
 - A scratch or void in the interconnection metallization, which reduces the width of the conducting strip by 50%
 - Any scratch or void in the metallization over a contact cut or window if the defect isolates more than 50% of the designed contact from the interconnecting metallization
 - Any scratch or void at, or over, an oxide step, which reduces the width of the conducting strip to less than 75% of the minimum width
 - Any device that exhibits bridged metallization defects so that the distance between any two metallization strips has been reduced to 25% of the designed separation
 - Any scribed chip that does not show 0.5 mil of SiO₂ between the interconnecting metallization pattern and the edge of the chip
 - Any device with a crack in the silicon chip that exceeds 1 mil in length and 3 μ m in depth and points toward an active area, metallization, or bond. Also, any device with cracks in the active circuit area or in the metallization area
 - Discolorations or stains in the top or bottom surface metallizations (Al and Ti/Ng/Ag).

- Polyimide or other passivation layer covering the IGBT top surface, with the exception of bonding pads (Any voids or opening in the layer with a size greater than 10×10 mils is a reject.)
- Any missing metallization in the bonding pads of more than 20%

The following is a list of possible suppliers of inspection equipment:

- SEM with backscatter and electron dispersion feature:
 - RJ Lee Instruments Ltd.
 - Princeton Gamma-Tech, Inc.
- Thermography tester:
 - Thermascan, Inc.
 - FLIR Systems
 - Image Therm Engineering, Inc.
 - Thermographic Measurements Co., Inc.
 - CMC Electronics
 - Advanced Thermal Solutions, Inc. (uses liquid crystal)
 - Advanced Research Technologies
 - Cedip Infrared Systems
- High-power 3D visual with video display:
 - Leica Microsystems
 - Nikon Instruments
 - Malcom Instruments Corp.
 - Hi-Scope Systems Co.
 - Mitutoyo America Corp.
 - Zeiss
- Solder wetting and tackiness tester:
 - Malcom Instruments Corp.
 - AST Products (contact angle system)
- X-ray system with 3D feature:
 - Agilent Technologies
 - FeinFocus
 - Phoenix X-ray
- Scanning acoustic microscope:
 - Sonix, Inc.
 - Sonoscan, Inc.
 - Honda Electronics Co., Ltd.

- Thermoacoustic:
 - ThermoSonix, Inc. (combines IR imaging and ultrasonic energy)
 - Indigo Systems
- Warpage tester/profilometer;
 - AkroMetrix
 - Veeco
 - Fisba Optik
 - Taylor Hobson Ltd.
 - Ambios Technology
 - MTI Instruments
 - KLA — Tencor
- Wire pull tester:
 - Dage Precision Instruments
 - Royce Instruments
 - Unitek Equipment
- Wafer and chip probing station:
 - Signatone
 - Cascade Microtech
 - Micromanipulator
- Plating thickness (x-ray fluorescent technique):
 - Veeco
 - Fischer Technology

4.2.3.2 Statistical Process Control

The object of statistical process control is to control parameters that cause variation. The usual practice in the power industry is to perform all go/no-go inspections and variable process controls on a sample basis. The sample here is a representative group selected randomly from the lot or run under inspection. The key concepts of sampling are:

- Random selection
- Sampling plan

4.2.3.2.1 Random Selection

Randomness ensures that the selected samples represent the entire lot. This is usually accomplished by assigning a number to each part in the lot and then applying the *Random Number Table* to select the random samples.

TABLE 4.16**Incoming Inspection**

Material	Inspection	Equipment/Technique
Substrates ^a (metallized ceramic, metal base plate)	Dimensions (with tolerance) Burr (≤ 2 mil) Warpage Surface roughness: Ridge Crack Scratch Groove Burr Content (purity) Plating (thickness, appearance, adhesion, solderability, wire bondability)	High-power 3D visual with display and scale Profilometer, Slit gauge test Optical profiling High power 3D, dye test " " " High power 3D, dye test Emission spectroscopy Visual (10–30 $\times$) stereo zoom X-ray fluorescent Blistering test (10 min at 300°C in H ₂) Wetting test; 2.5N pull test for 12 mil aluminum wire tape test
Chip (IGBT, FRED)	Visual crack (≤ 1.0 mil) Electrical (See Chart 4.1) Plating (top, bottom)	High-power 3D visual with display and scale Manual probing station Visual (10–30 $\times$), wire pull test, solder wetting test
Plastic case and cover ^a	Dimensions (with tolerances) Burr (≤ 2 mil) Chips, cracks, breaks Surface appearance Equal roughness Rz ≤ 12.5 nm Color uniformity Discolorization, stain	High-power 3D visual with display and scale
Terminals ^a	Dimension (with tolerance) Burrs, protrusion (≤ 2 mil) Nicks Scratches Grooves Dents Plating (thickness, appearance, adhesion, solderability)	High-power 3D visual with display and scale Visual (10–30 $\times$) stereo zoom X-ray fluorescent, tape test, wetting test

^a Specific details in [Chapter 5](#).

TABLE 4.17Near-Term Inspection⁷⁻¹⁰

Parameter	Site	Inspection	Equipment/ Technique
Solder	Presolder reflow (in-line automatic inspection or off-line sampling)	Uniformity Thickness Position Tackiness	High-power 3D visual with video display Tackiness tester
	Postsolder reflow	Smoothness ^a Uniformity (lumpiness) Continuity Cracks Coverage Wettability ^b	High-power 3D visual with video display 3D x-ray, SAM (Mil-883C) Wetting tester
Chip/ceramic/ metal baseplate attachment	Pre-/postsolder reflow	Placement Gross cracks	High-power 3D visual with video display
	Postsolder reflow	 Voids (< 10%) Hairline cracks Open Shorts Delamination Cracks Fissures	 SAM or 3D x-ray ^{c10} or thermoacoustic Dye penetrant test ⁶ (Zyglo test)
Wire bond	Post-wire bond	Crack, fracture, open, short Pull test	3D x-ray Wire pull tester 2.5-N pull test, 12-mil Al
		Bond size/shape	High-power 3D visual
Warpage Subassembly	Postsolder reflow	Bow Twist Warpage (Base plate warpage ≥ 75 μm, but not flat, slight concave upward; should be able to spin freely on a flat surface)	Optical shadow ^{7,8} Moiré ^{7,8} Profilometer

^a Pb-free solder joints are much duller and more grainy-looking than Pb solder joints.^b Wetting angle is 17 degrees for Sn/Pb, 36 degrees for Sn/Ag.^c Repeated x-ray inspections may cause damages to power chips. If this is the case, increase the distance between the sample and the tube focal point. Also, add filtration of about 100 μm thickness of zinc foil.

TABLE 4.18**Long-Term Inspection**

Parameter	Site	Inspection	Equipment/ Technique
Chip/substrate Attachment	Postsolder reflow	Hairline cracks Delamination	SAM or 3D x-ray or thermoacoustic
Solder joint microstructure ¹¹	Postsolder reflow	Intermetallics Grain size	SEM with backscatter and electron dispersion
		Crack Stress/strain Void	3D x-ray Moiré interferometry SAM
Thermography ^{6,12} (thermal mapping Thermal signature)	Post-wire bond	Hot spots	Infrared or liquid crystal Thermography Tester
Surface condition	Post-wire bond	Contaminants on chip surface — Cl, P, Na, K Residual passivation	Energy dispersive X-ray analysis Auger electron FTIR

4.2.3.2.2 Sampling Plan

This consists of sample size and the acceptance (or rejection) criteria. The sample size is a compromise between AQL, the acceptable quality level, and the cost to perform it. As defined by Mil-Std-105D, AQL is the maximum number of defects per hundred units. Unless otherwise specified, an AQL of 0.65 is acceptable for most production environments. The actual sample size can be obtained from the tables in Mil-Std-105D. For instance, for a lot size from 1 to 500, the relation between sample size and AQL is as shown in Table 4.19.

The acceptance (or rejection) criteria will depend on the parameters that are being monitored. Table 4.16 through Table 4.18 list the key parameters that should be monitored. It is, however, impractical and cost prohibitive to monitor all these parameters.

TABLE 4.19**AQL vs. Sample Size**

AQL (Level 1, Normal Inspection)	Sample Size (No Rejects Allowed)
0.10	125
0.25	50
0.65	20
1.0	13
1.5	8

The following guidelines can be applied to assist in selecting the appropriate parameters for monitoring. The parameter:

- Should be directly associated with product quality
- Should be easy to measure economically
- Should have high information content
- Should show measurable variation
- Should be chosen as one closely related to Pareto chart, which shows the frequency of various defects

The flow charts in [Section 4.4](#) show the parameters that are usually monitored in production. The following are some of these parameters with their typical acceptance criteria:

- Incoming inspection:
 - Substrates warpage (5 mils maximum)
 - Crack on IGBT/FRED chip surface (1 mil length, 3 μm depth maximum)
- Prerewflow:
 - Solder integrity (uniformity, thickness, coverage)
 - Chips/substrates placement (accuracy)
- Postrewflow:
 - Solder coverage and voids (maximum individual void: 5% chip area; total void: 10% chip area)
 - Wire-bonding integrity (pull test: 12 mil. Al, 2.5 N min., bond size: $1.2\text{ d} < \text{width} < 2.5\text{ d}$; $1.5\text{ d} < \text{length} < 5.0\text{ d}$. d = wire diameter)
 - In-line electrical testing: (I_{CES} , V_{CES} , I_{GES} , V_{GES} , V_{GETH} as specified)
 - Subassembly warpage: ($> 75\text{ }\mu\text{m}$ for baseplate convex towards heatsink)

Inspections and process control must be based on facts.¹³ Facts are obtained from data, which are either from physical measurements or from a nonmeasured entity such as counts and numbers. *These data must be real time and collected immediately after the process.* Control charts record and display collected data. There are six basic control charts, as shown in [Table 4.20](#).

Control charts contain control and specification limits. Control limits are the boundaries of the variation. Specification limits are external boundaries imposed by engineering on the parameters. Control limits are typically assigned as the ± 3 sigma limits from the centerline. *Control charts are used to detect variation.* An operation is considered to be stable and repeatable if its control charts have the following characteristics:

TABLE 4.20

Basic Control Charts and Usage

Chart	Usage
X Bar — Displays the variation, on average, of a series of measurements	Process control (Shewhart)
R — Displays the variation in the range of a series of measurements	
C — Displays the variation in the number of defects	Sample and final inspection
U — Displays the variation in the number of defects per unit	
P — Displays the variation in the fraction defective	
Np — Displays the variation in the number of defective units	

- The points are randomly distributed between the control limits.
- Most points are near the centerline.
- No points are beyond the control limits.

On the other hand, the characteristics of an unstable operation are:

- One or more points are outside the control limits.
- A number of successive points appear on one side of the centerline or the other.
- A long series of points is moving up or down without a change of direction.
- There is a cycle or pattern that repeats itself.
- There is an absence of points near the centerline.
- There is an absence of points near the control limits.
- There is a clustering of points in one area of the charts.

The process capability index, Cpk, is defined as

$$\frac{\text{specification limits} - \bar{x}}{\text{control limits } (3 \sigma)}$$

Cpk values of 1.33 or greater have become the accepted standard of well-controlled operations.

Any out-of-control operation should immediately trigger a process analysis, including cause-and-effect diagram, Pareto chart, and corrective action.

Numerous statistical analysis software programs can be used to display and analyze these data. One possibility is Prostat by Poly Software International (PSI).

Several other process control charts may be useful in monitoring specific situations:

- **Moving average ($\bar{x}$) chart** — This is good to monitor processes that change gradually, such as the reflow oven process.
- **CUSUM (cumulative sum) Chart** — This is good to monitor processes with small changes and an indication of when the changes occurred.
- **EWMA (exponentially weighted moving average) Chart** — This is good to predict process value for processes that may be drifting. It is mainly used in a preemptive mode to prevent a process from going astray.

Another statistical tool of interest is the concept of “six sigma,” which has been gaining popularity. A six-sigma system ensures product quality by measuring, analyzing, improving, and controlling the variability at the component and process levels.

In a six-sigma system, the number of defects is expressed in terms of parts per million (ppm). See Table 4.21.

As mentioned earlier, there are four key steps in the six-sigma process:

- **Measure** — Identify the key internal processes that affect the “critical to quality” characteristics. This phase is completed when one can count or measure the defects that affect quality.
- **Analyze** — Analyze the root cause that drives the defects. Use statistical tools to identify the key variables that are likely to be the most influential.
- **Improve** — Confirm the findings. Quantify the effects of these variables on the “critical to quality” characteristics.
- **Control** — Monitor and ensure that the key variables are within acceptable ranges.

TABLE 4.21

Number of Defects vs. Sigma Level

Status Level (σ)	Defects (ppm)
2	308,733
3	66,803
4	6,200
5	233
6	3.4

Finally, the statistical parameter that has been mentioned a lot lately is the defects per million opportunities (DPMO). This, however, is mostly used in measuring the manufacturing performance of printed circuit board assembly.

4.2.4 Long-Term Reliability

Even though the products are inspected during manufacturing for long-term reliability, the product must be designed for reliability (DFR).¹⁴

DFR consists of the following steps:

- Use of good design practices
- Reliable program planning
- Component parts derating
- Thermal analysis
- Component wear-out
- Failure modes and effects analysis (FMEA)
- Fault tree analysis
- Availability and system modeling
- HALT, HASS
- Design verification testing
- Product return rate analysis
- Failure reporting and corrective action (FRACA)
- Root cause failure analysis
- Internal process sharing and benchmarking

Following the six-sigma philosophy, long-term reliability should be addressed right at the initial design phase, established through HALT, maintained by HASS, and improved by failure analysis, followed by corrective actions.

In reality, the product is not only designed for reliability, but also must be designed for manufacturability, designed for testability, and designed for marketability. In other words, the product must be *concurrent engineered*.

The three key factors in long-term reliability are:

- Good design practices
- HALT and HASS
- Failure analysis

4.2.4.1 Good Design Practices

The module must be designed by using good, sound design practices that promote high performance and reliability. All the factors that can affect the lifetime must be identified and addressed. The lifetime of the module is determined by the following:

- Electrical/mechanical wear and tear
- Electrical aging

Electrical/mechanical wear and tear includes such mechanisms as temperature cycling, shock and vibration, switching transients, etc.

Electrical aging is the consequence of electrochemical processes, such as corrosion, formation of intermetallic compounds, electromigration, etc. These processes generally follow the chemical reaction relationship of Arrhenius:¹⁵

$$R_T = R_0 e^{-E_a/kT}$$

The activation energy, E_a , for the chemical reaction such as corrosion is typically 1.0 eV. Under this condition, every 9°C increase in temperature will double the reaction rate or aging, in other words, will halve the lifetime. It is therefore crucial to keep the reaction rate, R_T , and the wear and tear as low as possible.

These can be achieved by designing with good practices, such as the following:

- Lowering heat dissipation — Use fourth (or latest) generation IGBT
- Improving device ruggedness — Use IGBT with NPT structure
- Improving thermal coupling — Use solder, insulating substrate, and metal baseplate with good thermal conductivity
- Lowering heat sink temperature — Use air flow or water coolant system
- Lowering the reaction rate — Use high-purity silicone conformal coating or parylene coating and epoxy resin to protect chips from the environment
- Reducing mechanical wear and tear — Use matching TCE material to reduce stress
- Avoiding electromigration — Operate within current density of 10^6 A/cm²
- Reducing chip breakdown — Specify within the chips' maximum ratings and derate to 85%
- Reducing intermetallics formation — Use compatible metals, such as Al wire to Al metallization; use proper solder and optimize reflow profile

- Reducing Al wire lift-off — Operate within specified Tj; optimize bonding
- Lowering voltage overshoot — Reduce stray inductance

4.2.4.2 **HALT and HASS**

HALT and HASS are tests that rely on the concept of logarithmic time compression, applying much higher stress than is expected to exist in the end user's environment.^{14,15,17,18}

- **HALT (highly accelerated life testing)** — To establish the operating and destruct limits of the product through a step series of stress/fail/fix testing during the design and engineering phase
- **HASS (highly accelerated stress screen)** — To trigger and screen out the product's infant mortality, which may be introduced during the manufacturing process and through vendor parts

HALT precedes HASS. *HALT is performed during the design stage* to establish the fundamental operating and destruct limits of the products.

HALT involves the following steps:

- Apply environmental stress in steps (for example, temperature cycling step $\pm 10^{\circ}\text{C}$ starting at 0 to 70°C , vibration steps of 5 G starting at 0 G, or humidity steps of 5% starting at 30% and 1.2 Atm or other combination, with or without power applied) until the product fails.
- Analyze, change, and fix the failure. (This may involve a change in material, process, or equipment.)
- Step-increase the stress until the product fails again.
- Analyze, change, and fix again.
- Repeat this stress/fail/fix process.
- Establish the operating and destruct limits. (The operating limit is the limit beyond which the product will not operate correctly; the destruct limit is the limit beyond which the product is destroyed.)

HASS testing limits are selected from HALT data. *HASS is performed during production stage.* HASS is usually performed on a 100% basis during the initial production phase and may be extended to once a month at the later stage, in which case it becomes highly accelerated stress auditing (HASA). HASS contains the following:

- Precipitation screen to find latent defects
- Detection screen to find patent defects

- Failure analysis
- Corrective actions

HALT and HASS tests have proved to find latent defects that would very likely precipitate during users' applications, causing product failures in the field. As a result, the HALT and HASS testing can greatly improve product reliability.

The limits for both screens (precipitation and detection) are selected so that they are outside of the tails of the distribution of the failure modes that define the operating and destruct limits. In other words, these limits represent the highest possible stresses without weakening the product. The selection of these limits is an interactive process. To test whether these limits are effective, a rule of thumb is to run a sample group through the screens 10 times. If no defects are found or if there are excessive failures, the limits need to be reset.

An effective profile for HASS is the combination of temperature cycle and vibration. For instance, a precipitation screen may consist of five cycles from -65 to 165°C , followed by five cycles of detection screen from -50 to 150°C , superimposing on both screens a 10-G vibration. (This profile serves only as an illustration and is not intended to be used in actual screening.)

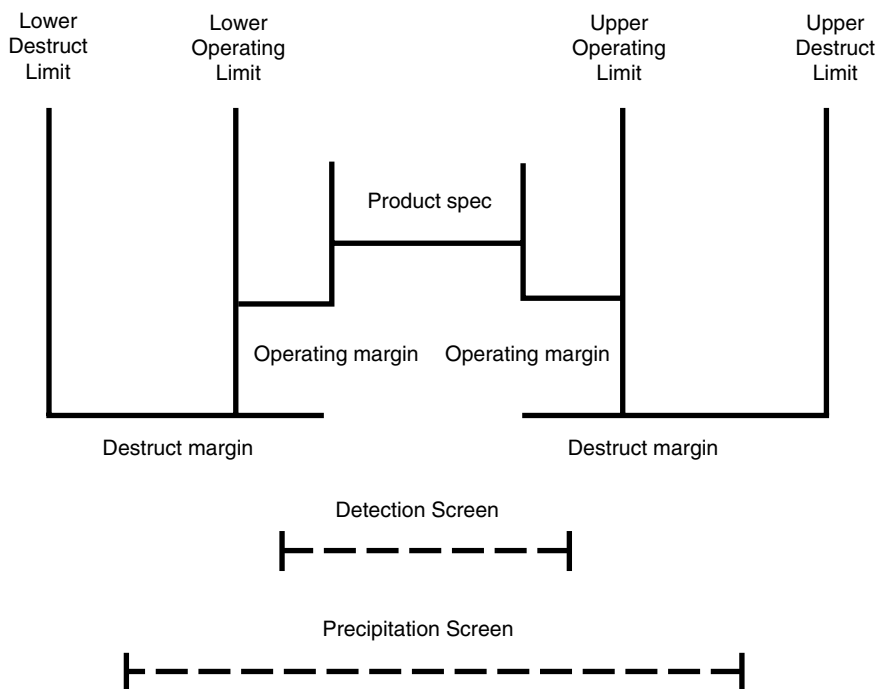


FIGURE 4.8
HALT and HASS limits.

The following is a list of possible suppliers for HALT/HASS systems:

- Environmental Screening Technology
- Envirotronics
- Thermotion Industries
- ESPEC

4.2.4.3 Life Tests

After performing the HALT/HASS, the power module should be capable of passing the following life tests:^{15,16,19}

1. High-temperature reverse bias (HTRB):
 - Output
 - 125°C for 1000 h at rated output voltage
2. High-temperature gate bias (HTGB):
 - Input
 - 125°C for 1000 h at rated gate bias
3. Screw torque/fast-on tab durability:
 - Output main screw
 - 2× rated torque for 336 h (1.96 N-m for M5 and 2.94 N-m for M6)
 - Durability of fast-on tab: 25 repeated insertions/withdrawals
Insertion force — 4.5 Kg; withdrawal force — 4.5 Kg
4. Temperature cycling:
 - -40 to 125°C for 50 cycles
 - 30 min ramp/dwell
 - 2-h cycle time
5. Temperature/humidity resistance:
 - 60°C/90% RH for 1000 h
6. High-temperature storage:
 - 125°C for 1000 h
7. Low-temperature storage:
 - -40°C for 1000 h
8. Power cycling — Combined environmental–power test²⁰
 - Power on — At rated current
 - Power off — At rated voltage
 - -40–90°C at 90–95% RH
 - 8 h per cycle
 - Total — 125 cycles

9. Mechanical shock (only for mobile applications):
 - 500 G for 1 ms at X, Y, and Z directions (three times each)
 - (or 20 G for 20 ms at X, Y, and Z directions)
10. Mechanical vibration (only for mobile applications):
 - 10 G for 6 h at X,Y, and Z directions
 - Frequency — 100 Hz through 2 kHz
 - Sweep time — 20 min per cycle
11. Plastic case stress test:
 - Mount the module
 - Apply force of 50 lb to each side

Table 4.22 presents the defects detected by these testings. Key parameters are monitored pre- and post life tests. Table 4.23 shows the acceptable shift in the specification limit of these parameters.

4.2.4.3.1 Failure Rate

The failure rate of a reaction generally follows the Arrhenius equation:²²

$$F = A \exp (-E_a/kT) \quad (4.1)$$

where

- F = Failure rate
- A = A constant
- E_a = Activation energy, eV (~ 0.7 to 1.3 eV)
- k = Boltzmann's constant (8.6×10^{-5} eV/k)
- T = Absolute temperature, K

Because the life test is performed at increased temperature, an acceleration factor, a , can be defined as

$$\left[\frac{E_a}{k} \left(\frac{1}{T_N} - \frac{1}{T_L} \right) \right] \quad (4.2)$$

where

- T_N = Normal operating temperature
- T_L = Life-test temperature

TABLE 4.22

Test	Defects Detected by the Test
High-temperature reverse bias (HTRB)	Degradation of breakdown characteristics due to foreign materials and polar/ionic contaminants disturbing the electric field termination structure Surface and metallization faults Wire-bond defects
High-temperature gate bias (HTGB)	Breakdown of the gate oxide due to localized thickness variation Particulates in the oxide Channel inversion due to mobile ions in the oxide Wire-bond defects
Temperature cycling (thermal shock)	Thermal fatigue of chip/ceramic, terminals/ceramic, and ceramic/metal baseplate interfaces due to heating and cooling, causing performance degradation Wire-bond and solder fatigues Thermal shock (a faster transition between hot and cold temperatures) is more effective in detecting wire fatigue; temperature cycling (a slower transition) will reveal more solder fatigue
Humidity	Degradation of electrical leakage parameter due to moisture penetration Corrosion and chemical reactions
Power cycling	Thermal fatigue of chip/ceramic, terminals/ceramic, and ceramic/metal baseplate interfaces due to heating and cooling, causing performance degradation
Mechanical shock/vibration	Loose parts Wear and tear Solder joints Fatigue/wire-bond defects — flexure, crack Chip attachment defects Mechanical faults
High-/low-temperature storage	Contact defects Moisture ingress Oxidation Metallization defects Thermal aging Physical changes Wire-bond defects — intermetallic, Kirkendall voids

TABLE 4.23

Monitoring Parameters after Life Tests

Parameter	Acceptable Shift in Specification Limit (%)
I_{GE}	No change
V_{ISO}	No change
V_{GETH}	± 20
V_{CESAT}	+20
I_{CES}	+20
V_F	+20

If n modules are life tested at temperature T_L for t hours, the equivalent total device hours at normal operating temperature, T_N is ant , and if x units failed during life test, the failure rate at T_R is x/ant .

This is usually expressed in $\%/1000$ h or FIT, where $FIT = 1$ failure/ 10^9 h.

A confidence factor, C , also must be assigned to this estimate. The higher the confidence level, the higher the failure rate will be. The failure rate becomes

$$Cx/ant \quad (4.3)$$

Typically, a 90% lower confidence limit is adequate. This means that 9 out of 10 times, the failure rate will be lower than that given by Equation 4.3. Table 4.24 shows the confidence factor for a 90% lower confidence limit.

For industrial applications, a failure rate of 100 FIT at normal operating temperature is acceptable. More details can be obtained from the following documents:

- Mil-S-19500
- Mil-M-38510
- Mil-Std-883C
- Mil-Std. 202
- Mil-HDBK-217E

TABLE 4.24

Confidence Factor for a 90% Lower Confidence Limit

x	C
0	2.3
1	3.9
2	5.3
3	6.7
4	8.0

4.2.4.4 **Failure Analysis**^{15,16}

Failure analysis is an essential element of the production line and must be performed on a regular basis. It is an integral part of reliability engineering. The key features to failure analysis are:

- Identify the problems
- Establish proper techniques and instrumentation to determine possible causes:
 - Study case inputs and process control data
 - Inspect visually as is (mechanical damage, other external defects)
 - Use x-ray imaging – transmission (wire-bond failure, chip crack, solder open/short)
 - Use microprobe electrical test
 - Decapsulate case and cover. Remove epoxy and silicone coating if necessary (e.g., by chemical means such as Dynasolve solvent)
 - Use 3D power visual with video display (open/short, corrosion, electro-migration, stain, ESD)
 - Examine optical profile (excessive warpage)
 - Use infrared microscopy (hot spot, void-induced or thermally induced failure)
 - Use Scanning Acoustic Microscoping (C-SAM) (solder defect, chip/substrate crack)
 - Do dye penetration test (crack)
- Ensure speed of response in determining whether the root cause is:
 - Manufacturing related
 - Component-supplier related
 - User related
- Run tests to verify proposed corrective actions
- Implement corrective actions in manufacturing
- Validate corrective actions
- Communicate all reports electronically
- Complete final report within 10 days of initial response (goal)

Table 4.25 through Table 4.27 show some common failure mechanisms in a power module. Certain useful equipments for failure analysis such as precision sawing, cross-sectioning, and decapsulation are supplied by Ultra Tec.

TABLE 4.25

Common Failure Problems due to Manufacturers

Cause	Examples of Failures
Material problem	Mismatching of coefficient of thermal expansion Chemical interactions or incompatibility among different materials in contact
Processing problem	Chip degradation during process Chip attachment defects — cleaning, solder, gas, oven Wire-bonding defects Coating defects Mechanical defects, cracks, dents, scratches, etc.
Thermal problem	Destruction or degradation due to thermal expansion mismatch Destruction or degradation due to excessive T_j , caused by poor solder attachment or material selection
Electrical problem	Chip or package destruction due to isolation voltage failure Soft leakage current due to gate oxide/dielectric contamination
Mechanical problem	Damages of terminals due to bending/opening/breaking Package cracking
Chemical problem	Corrosion of chip metallization Corrosion/rusting of terminals
Moisture problem	Corrosion/chemical reaction Degradation of leakage current
ESD problem	Latent damages, with microcracks or defects dormant until aggravated by environmental stressing
Transportation problem	Module not sufficient by protected reading to package damage and terminals bending or breaking

TABLE 4.26

Common Failure Analysis due to Component Suppliers

Cause	Examples of Failures
Material problem	IGBT gate oxide latent defect — crack IGBT/FRED passivation dielectric latent defect Chip testing errors Plating defects leading to corrosion on metal baseplate and terminals; poor solder attachment; weak wire bonding DBC metallization processing defects Solder material defects

TABLE 4.27

Common Failure Mechanisms due to Users

Cause	Examples of Failures
Electrical problem	Outside RBSOA — excessive current; excessive voltage Gate overvoltage — ESD; gate wiring too long
Thermal problem	Excessive $T_j - V_{CESAT}$ due to insufficient gate drive; overcurrent due to shorting, protection failure; excessive switching loss; excessive contact loss; excessive case temperature
Mechanical problem	Excessive force in attaching bus bar to terminals Excessive force in repeated insertion to fast-on tabs Excessive force in mounting the module to heat sink
Storage problem	Corrosion/chemical reaction due to humidity Contact problem due to dust ESD problem due to lack of or insufficient protection

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-

4.3 Manufacturing Facilities

Certain requirements are imposed on the production facilities in order to:

- Avoid damages caused by electrostatic discharge (ESD)
- Achieve void-free, high-yield assembly
- Produce a highly reliable power module product
- Satisfy safety and environmental requirements

These requirements involve:

- ESD
- DI water
- Processing gas
- Chemicals
- Electrical supply
- Relative humidity
- Air-flow and pressure differentials
- Room particle count
- Storage cabinets
- Cleanroom accessories and details
- Safety standards
- Environmental requirements

4.3.1 ESD¹

ESD is a serious threat to the MOS-gate type of devices. It creates damage by causing either an excessive voltage stress or an abnormally high current discharge, resulting in catastrophic failure or performance degradations, which are *latent defects* that may surface later during operation. Studies have found that ESD losses are about 6.5% of annual revenues, which implies that the global electronics industry is losing in excess of \$84 billion every year. ESD must therefore be controlled. Controlling ESD-induced damages requires observing appropriate precautions during the following:^{2,3}

- Handling of components
- Testing
- Assembly
- Shipment
- Field of operation

The following is a list of precautions that should be observed during assembly:

- Subassembled parts and finished products should be stored in an antistatic environment.
- All equipment should be properly grounded, especially the tips of the die bonder, wire bonder, dispenser, and soldering tools.
- All operators should wear antistatic wrist bands with proper grounding and antistatic footwear in assembly areas.
- Higher humidity conditions provide a means to discharge any built-up static electricity but must be within the comfort zone of operators. Maintain at 40 to 60% RH.
- Use air ionizers to neutralize charge buildup. This is most efficiently done by using a low-pressure, low-flow air blower. An air ionizer is a must for the assembly of MOS-gate type devices.
- Do not use tools with plastic handles. All tools must be constructed with static-safe materials.
- The floor and all surfaces of working benches must be covered with static dissipative material to prevent generation of static electricity. Surface resistivity for these materials should be between 10^5 and $10^8 \Omega/\square$. One possible coating for hard floor is Statguard static-dissipative floor finish, by Charles Water.
- Products should be shipped in an antistatic bag or package.
- Avoid touching the terminals with bare hands.
- Unused terminals should be covered with static-dissipative material.
- Clean using an antistatic, prewetted wiper.

The following specific precautions must be taken when handling the finished IGBT module:

- Store and transport in closed bags or containers made of conductive and antistatic material.
- Ionize the N₂ gas in the storage bags or containers.
- Do not remove the conductive sponge or tape mounted between the gate and the emitter before starting operation.
- Ground via a high-value resistor (between 100 k and 1 meg ohm) when handling the module. Do not touch the gate terminal.
- Ground any parts, such as tools or workbench, that the IGBT module may touch.
- Check that any residual electric charge in the measuring equipment has been removed before testing the IGBT module. Apply voltage to each terminal, starting at 0 V and return voltage to 0 V when finishing.

Note: All operators working in the ESD areas must be trained and periodically tested.

4.3.1.1 Test Schedule for ESD-Controlled Products

ESD-controlled products must be tested on a strict, regular basis to ensure that they are functioning properly.^{4,5} Table 4.28 shows how often these ESD-controlled products should be tested to ANSI/ESD S20.20, ESD STM7.1, and STM 97.1 for floors.

TABLE 4.28

ESD Testing Schedule

Frequency	Items
Daily	Wrist straps, footwear, smocks (properly worn) Whenever possible, it is preferable to have continuous real-time monitors that will automatically alarm if the ESD performance is out of safe specifications ⁵
Weekly	Workstations, floor mats, ESD ground connections
Monthly	Static surveys of ESD protective areas and smocks (electrical tests)
Quarterly	RTG (resistance-to-ground) of work surface and floor, wrist strap monitor, ESD ground continuity
Semiannually	Ionizer balance and charge decay Operator testing
Annually	ESD system compliance with the ESD control plan

4.3.1.2 ESD Audit^{4,6}

The auditing process is the binding force behind the entire ESD control program. It assures the company management and customers that the ESD is under control.

MIL-HDBK-263, Section K, presents a checklist to use in performing an ESD audit. It provides more than 500 specific subjects to inquire into and investigate during auditing. The checklist should be tailored to the specific requirements of the ESD control program. Effective auditing should revolve around the following factors:

- Written and well-defined standards and procedures must exist.
- One must possess specific instrumentation for measuring and collecting data.
- Audits must include all areas:
 - Receiving
 - Inspection
 - Warehouse
 - Assembly
 - R&D
 - Shipping
 - Offices
- Audits must be frequent and regular. A recommended frequency is six times per year.
- Maintain trend charts and detailed records and prepare reports in compliance with ISO-9000.
- Corrective action must be implemented.

4.3.2 DI Water

- By ASTM standards, DI water should be 16 meg ohm minimum at 25°C.
- Maximum number of particles: 100/cc; maximum particle size: 0.50 μm .
- The latest trend is to use ozone-DI water with ozone concentration of about 30 to 50 ppm. This is effective in the removal of organic contamination.

4.3.3 Processing Gas

- N₂ processing gas should contain < 100 ppm of O₂, 5 ppm of moisture.
- Gas purity, O₂, H₂, Ar — 0.99999
- Line pressure, N₂, O₂ — 5–6 bar
- Compressed air — 10 bar

4.3.4 Chemicals

- HNO_3 — 60 to 65% concentration
- HCl — 35%
- HF — 50%
- H_3PO_4 — 80 to 85%
- CH_3COOH — 90 to 95%

4.3.5 Electrical Supply

- $115 \text{ V} \pm 5\%$
- $60 \text{ Hz} \pm 2\%$
- Stand by UPS

4.3.6 Relative Humidity

- 40 to 60% at 20°C

4.3.7 Air-Flow and Pressure Differentials

- Air should enter the room through supply registers and exit the room through return ducts as smoothly as possible. This will reduce turbulence, eddies, and dead spaces.
- Positive air pressure must be maintained in the cleanroom, thereby protecting the cleanroom classification. A pressure differential of 0.05" water column is sufficient.

4.3.8 Room Particle Count

- Air particle count is an early warning indication for possible room contamination.
- Particle count in the processing area should be $\leq 100,000$. Avoid "over-design." (Plastic curtains, modular cleanroom, or laminar hood should be $\leq 1,000$.)
- Activated carbon, UV, and HEPA filters should be installed in the processing room.

4.3.9 Storage Cabinet

4.3.9.1 *Passive Parts and Tools*

There are two types of storage cabinets, both ultradry and at class 1000:

- Using N₂ gas, containing less than 5 ppm of moisture
- Using recycled zeolite desiccant and no N₂ gas

4.3.9.2 *Power IGBT/FRED Chips, Subassembled IGBT Parts, and Finished Modules*

- Antistatic
- 40–60% RH at 20–25°C
- Class 1000

4.3.10 Cleanroom Accessories and Details⁷

All cleanroom accessories and details should comply with cleanroom standards (209E, ISO 14644):

- Furniture — Benches, chairs, racks.
- Apparel — Garments, gloves.
- Air shower.
- Floor mats — Such as Dycem polymer flooring.
- Cleaning wipes — Use wipers made from hydroentangled polyester cellulose and prewetted with semiconductor grade isopropyl alcohol (IPA), such as those offered by Anticons and Texwipes. Otherwise, the wiping solution should be DI water with 6 to 9% IPA. The prewetted wipers are used mostly in solder printing rework. For coating and case/lidding operations, use dry wipes.
- Cleaning accessories — Use flat surface mop with polyester-knit head.
- Details:
 - Cleaning schedule, such as top-down super clean, continuous cleaning, etc.
 - Operator training program.

4.3.11 Safety Standards⁸

All safety regulations must comply with UL safety standards and OSHA's General Industry Standards (29CFR Part 1910). Important areas include:

- Fire alarm and sprinkler system
- Storage and transport for flammable and toxic materials
- Hoisting equipment
- Electrical safety
- Fume exhaust system/ventilation system
- Medical and first-aid support

4.3.12 Environmental Requirements

All environmental regulations must comply with OSHA, EPA, and ISO 14000 standards. Special efforts should focus on the following:

- Management of cleaning residues, solvents, and hazardous waste materials
- Elimination of ODC production

The following is a list of possible suppliers for ESD accessories, prefabricated cleanroom storage cabinets, particle counters, and cleanroom accessories:

- ESD accessories:
 - General:
 - SIMCO
 - 3M
 - Charles Water
 - Desco
 - Assembly Tray:
 - HMS Compounds
 - Packaging:
 - SECO
 - Stat-tech
- Prefabricated modular cleanrooms:
 - Clean Air Technology, Inc.
 - Air Control, Inc.
 - American Cleanroom Systems
- Laminar hoods and cleanbooths:
 - Terra Universal
- Storage cabinets:
 - Terra Universal

- Seika Machinery, Inc.
- Clean Air Products
- Toyo Living Co., Ltd.
- Particle Counters:
 - RION
 - ART 1
 - Pacific Scientific Instruments
- Cleanroom accessory distributors:
 - Terra Universal
 - Liberty Industries
 - Nerak
- Trace moisture analyzers for N₂ gas:
 - Tiger Optics
- Trace oxygen analyzers for N₂ gas:
 - PBT Dansensor

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4.4 Manufacturing Flow Charts

In this section, two different manufacturing processes are presented for comparison.

4.4.1 Standard Manufacturing Process

- Solder attachment of chip/ceramic, power terminals/ceramic, and ceramic/baseplate by reflow in forced-air convection or infrared conveyor oven. The more complex three-solder process is presented. The commonly used two-solder process is obtained by simply combining MP6 and MP9 into a single reflow step.
- Aluminum-wire bonding
- Coatings:
 - First — Silicone gel
 - Second — Epoxy
- Process control
- Testing

4.4.2 Alternative Manufacturing Process

- Solder bump IGBT and FRED chips
- Solder attachment of chip/ceramic, chip-power electrodes/ceramic, power terminals/ceramic, and ceramic/baseplate by reflow in single-chamber or vacuum oven.
- Coatings:
 - First — Silicone gel or parylene
 - Second — Epoxy
- Process control
- Testing

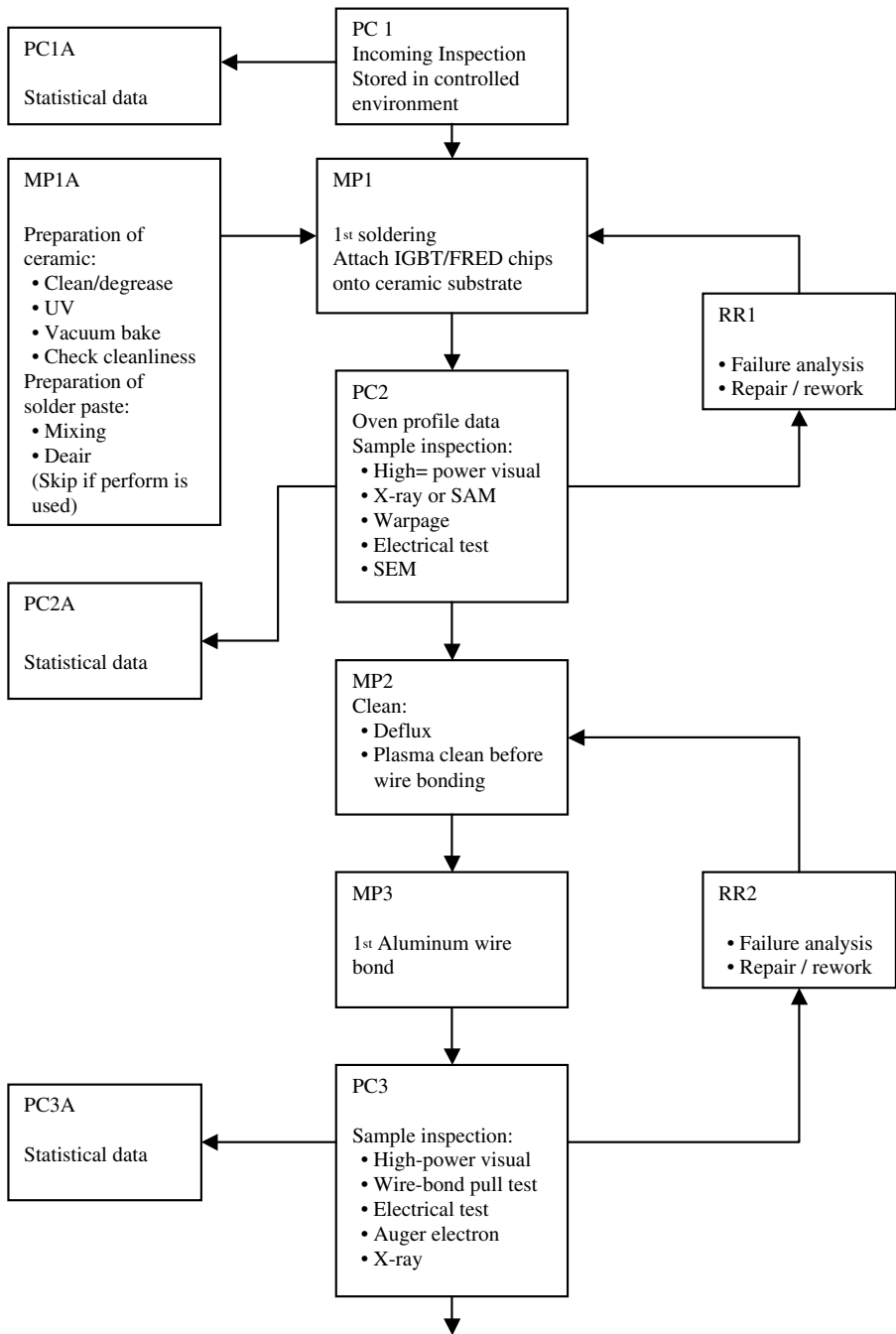


CHART 4.3A
Standard manufacturing process.

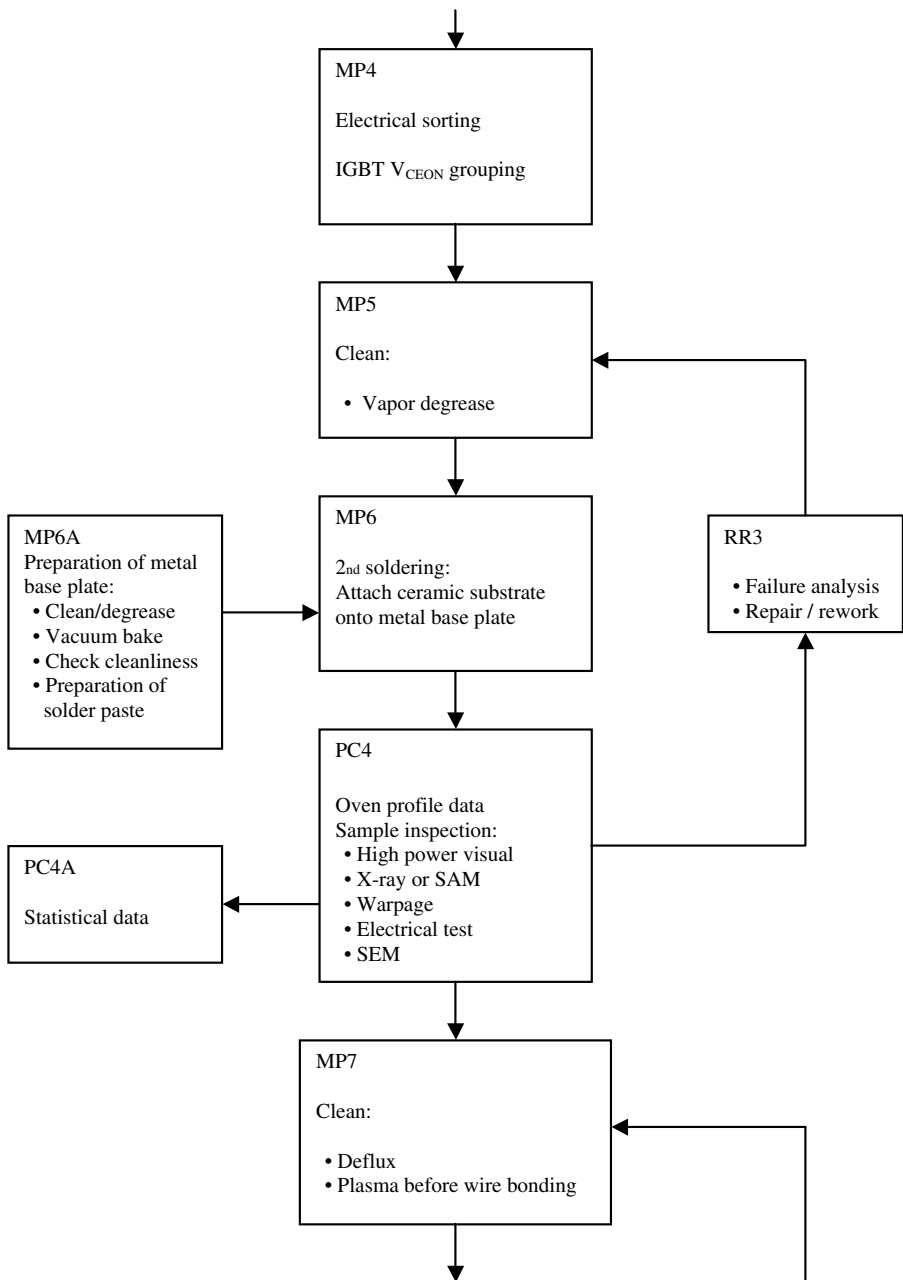


CHART 4.3B

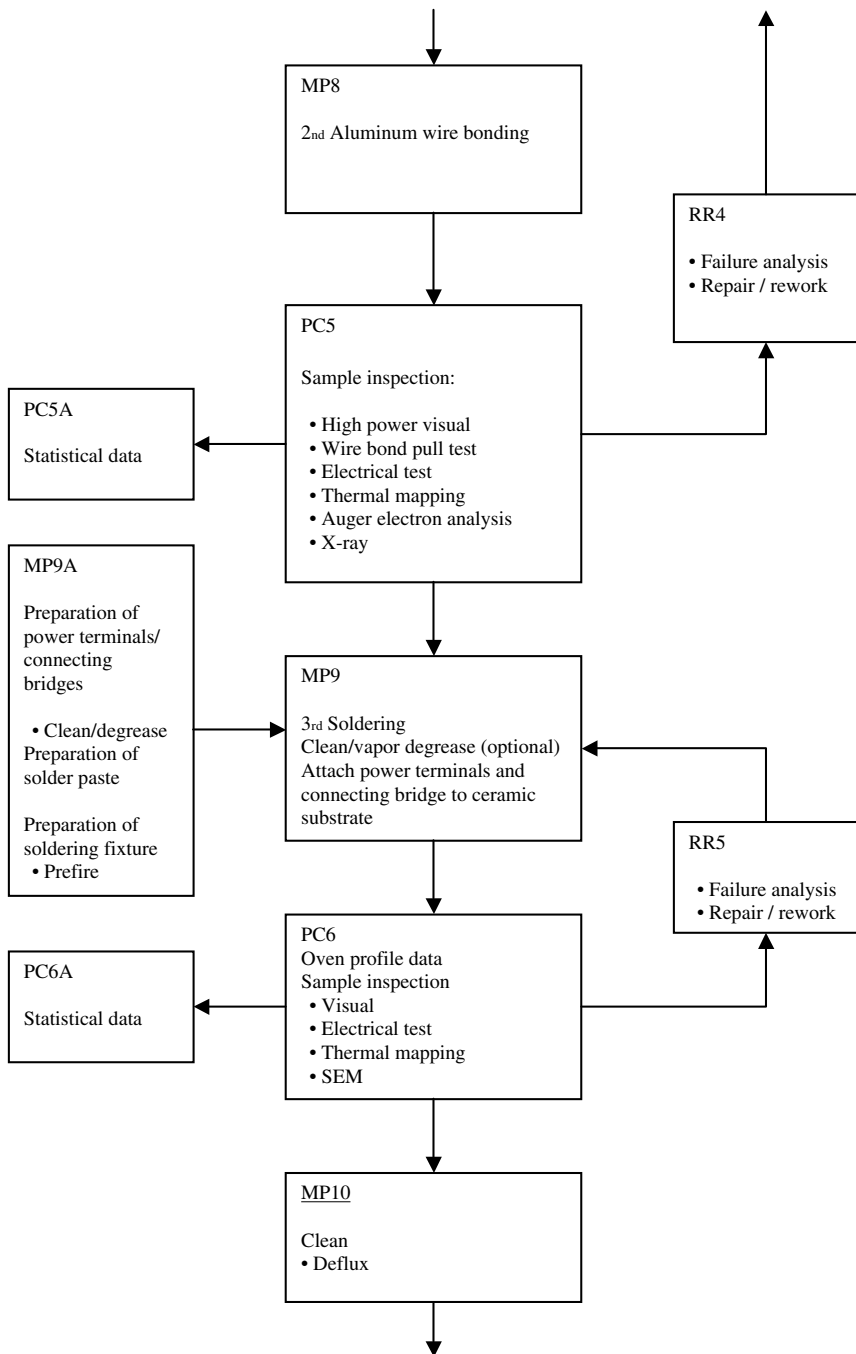


CHART 4.3C

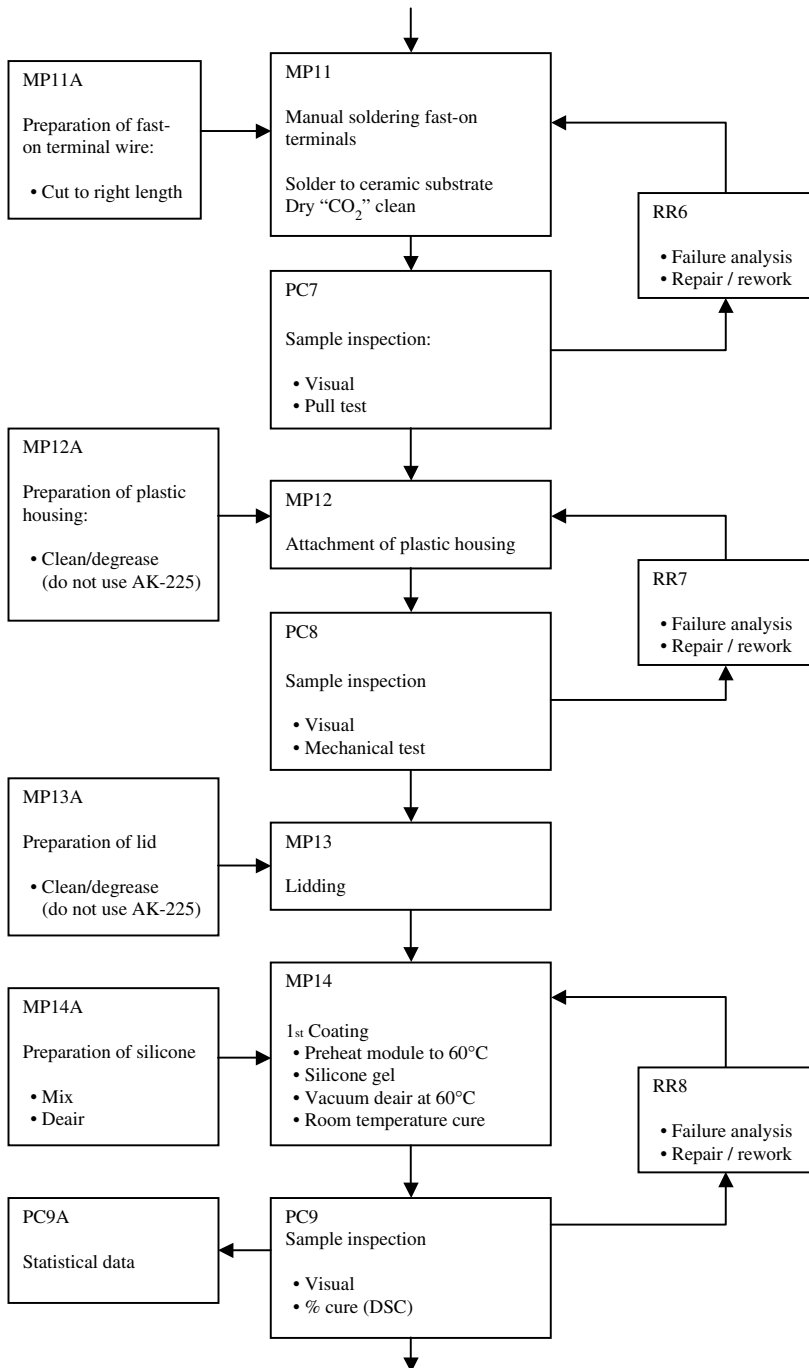


CHART 4.3D

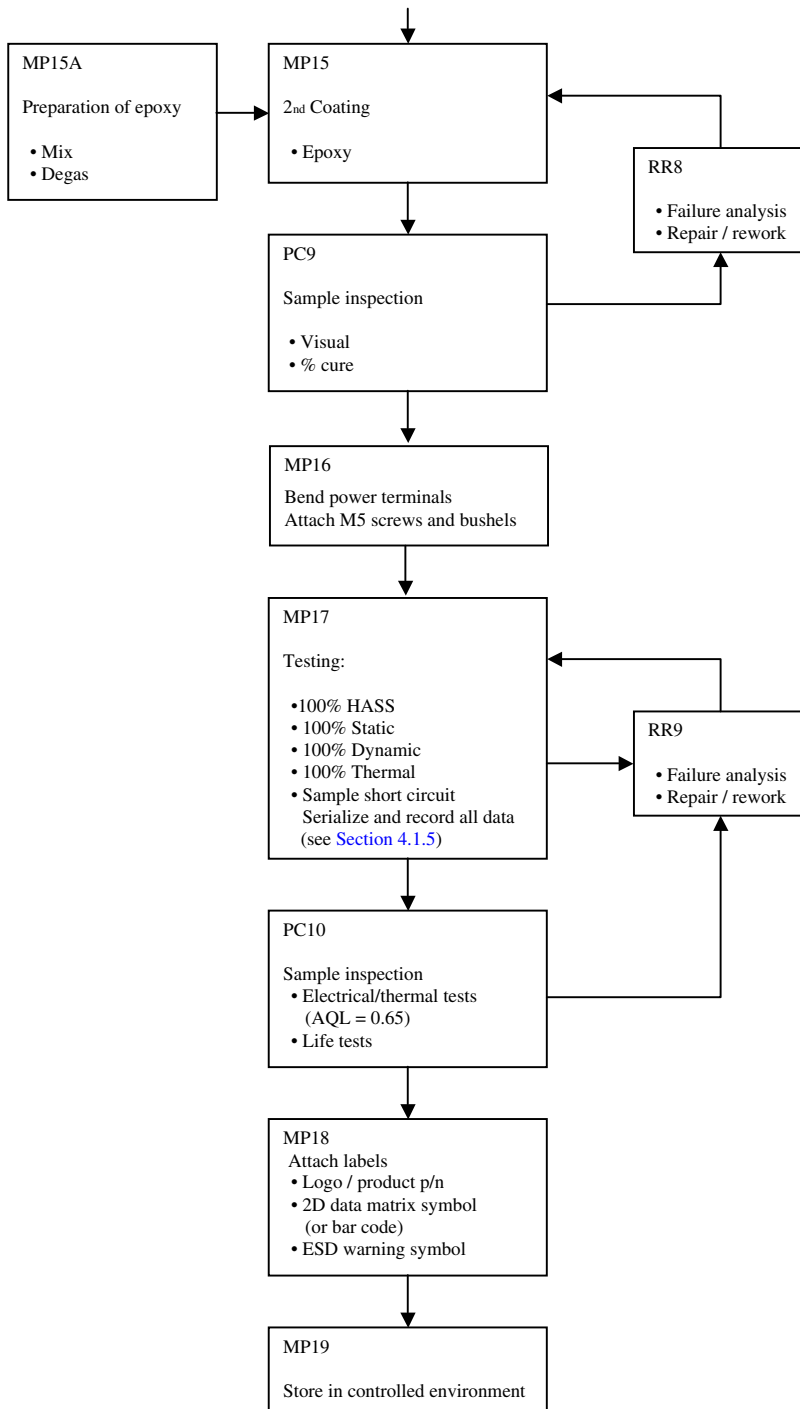


CHART 4.3E

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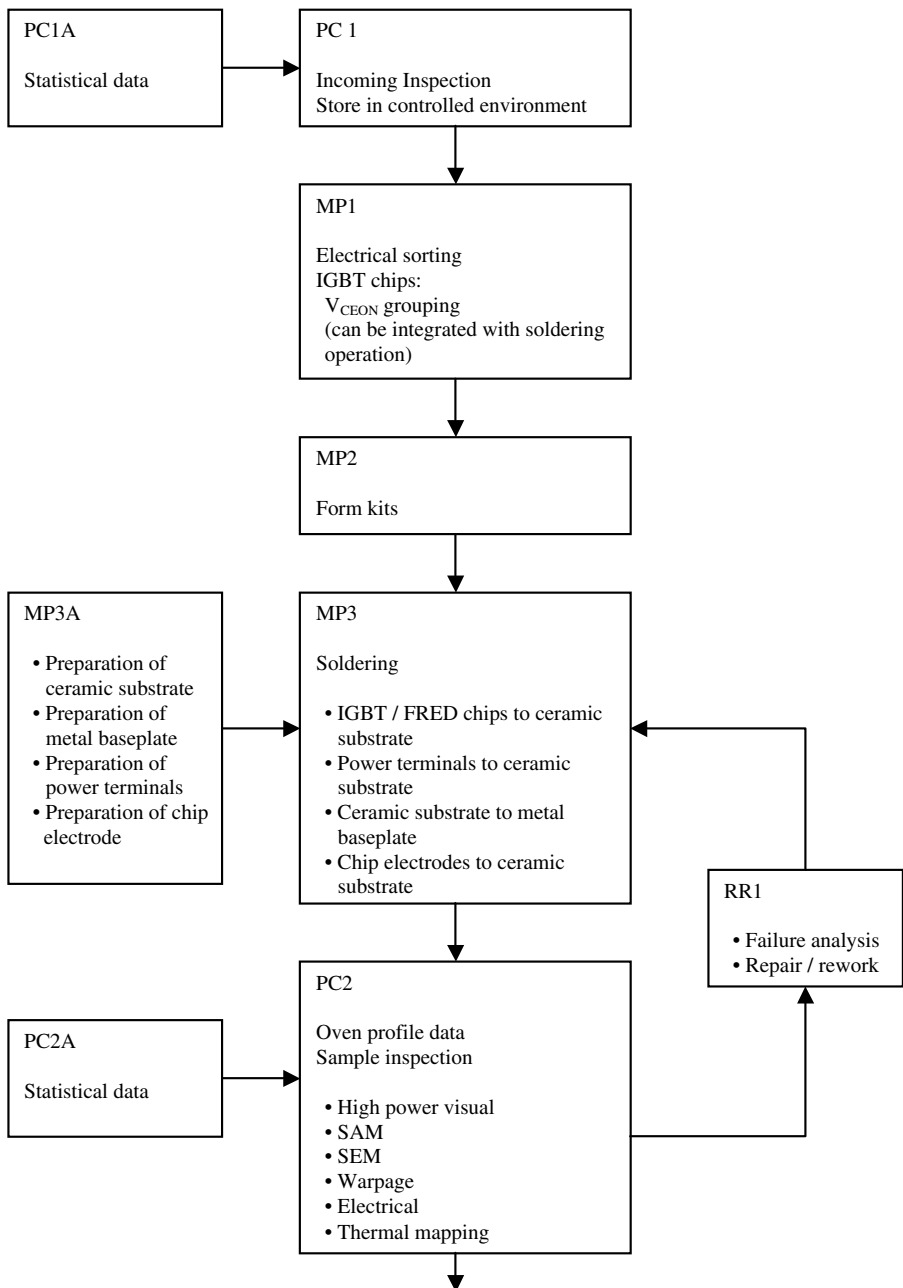


CHART 4.4A

Alternative manufacturing process.

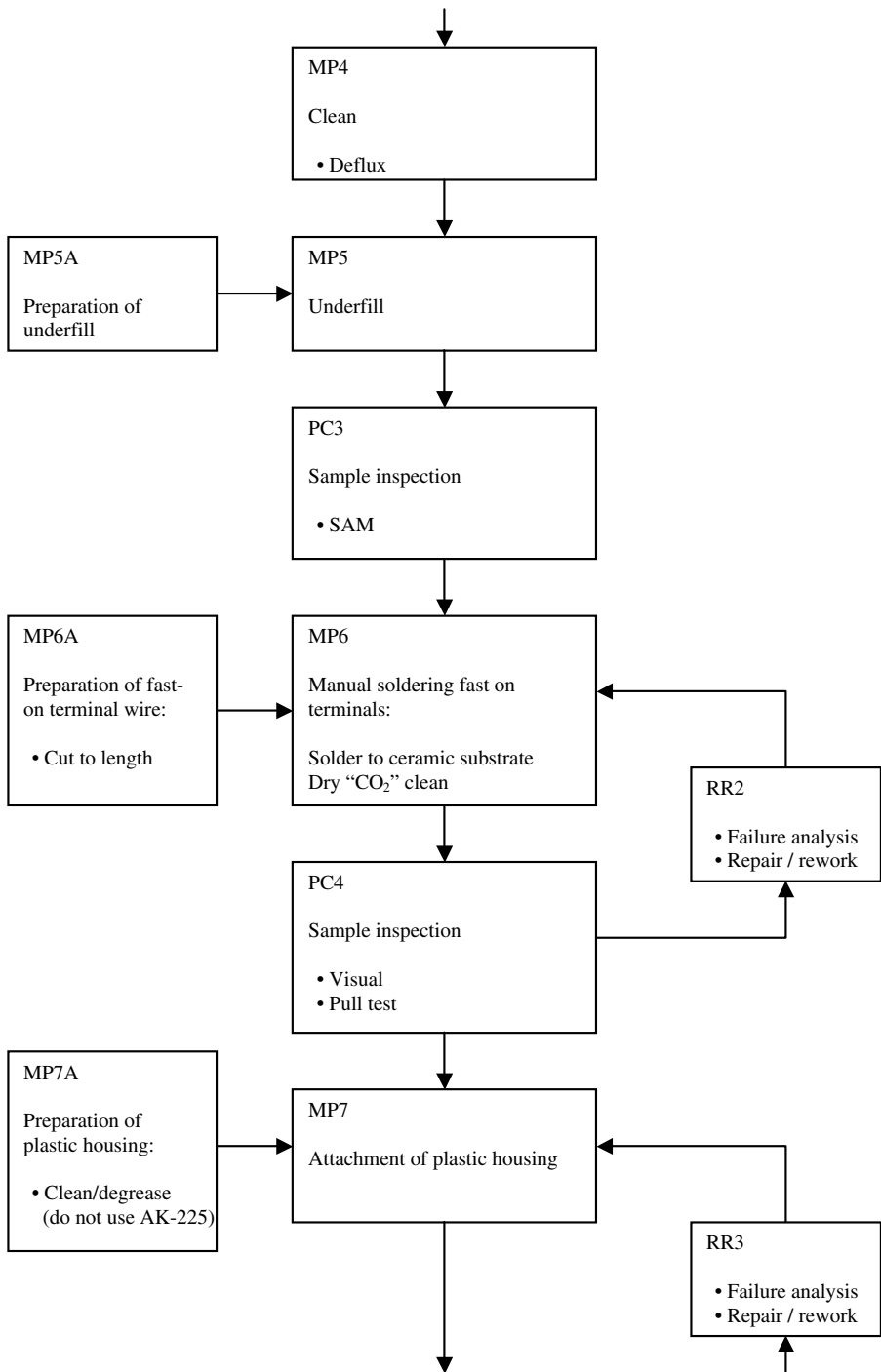


CHART 4.4B

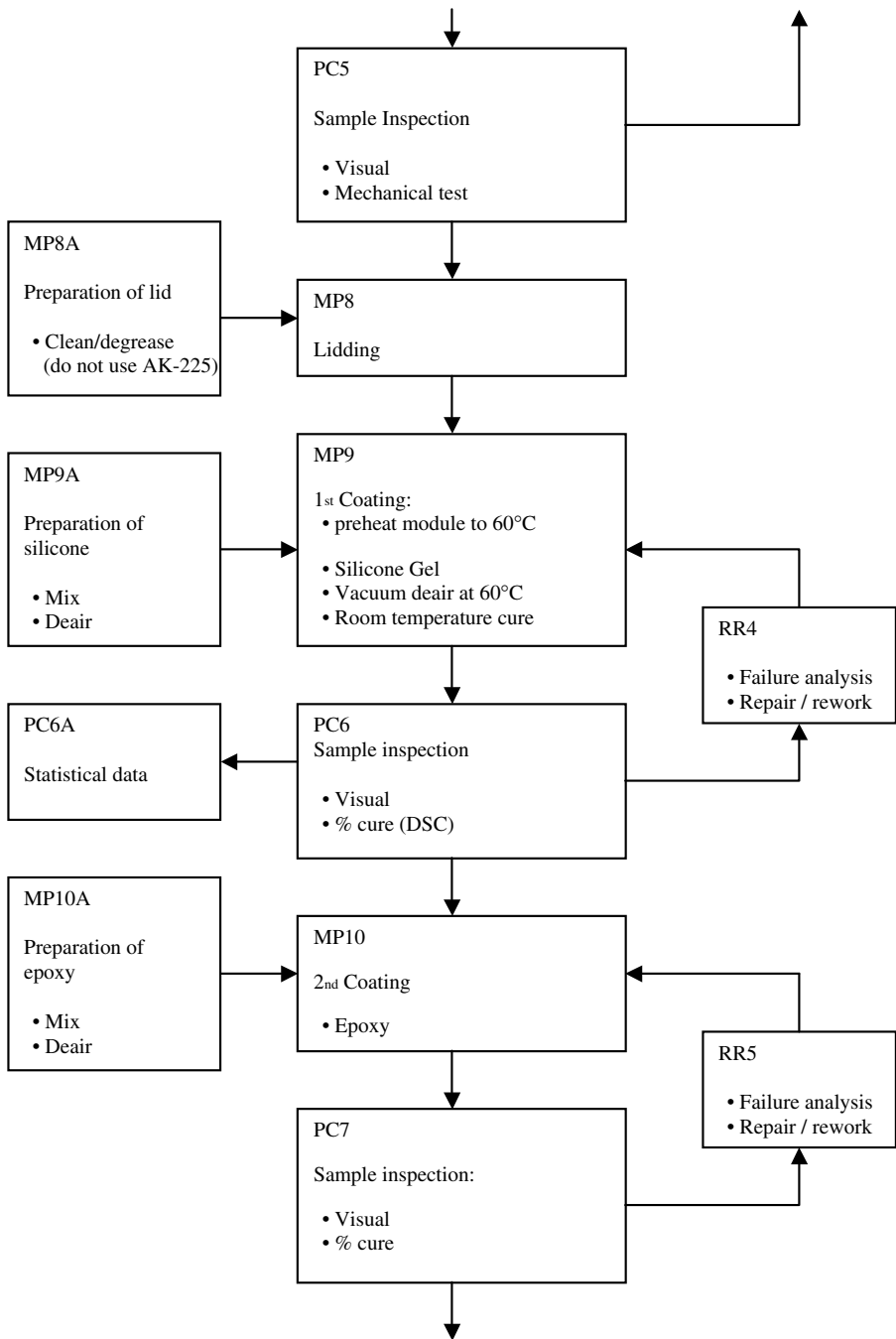


CHART 4.4C

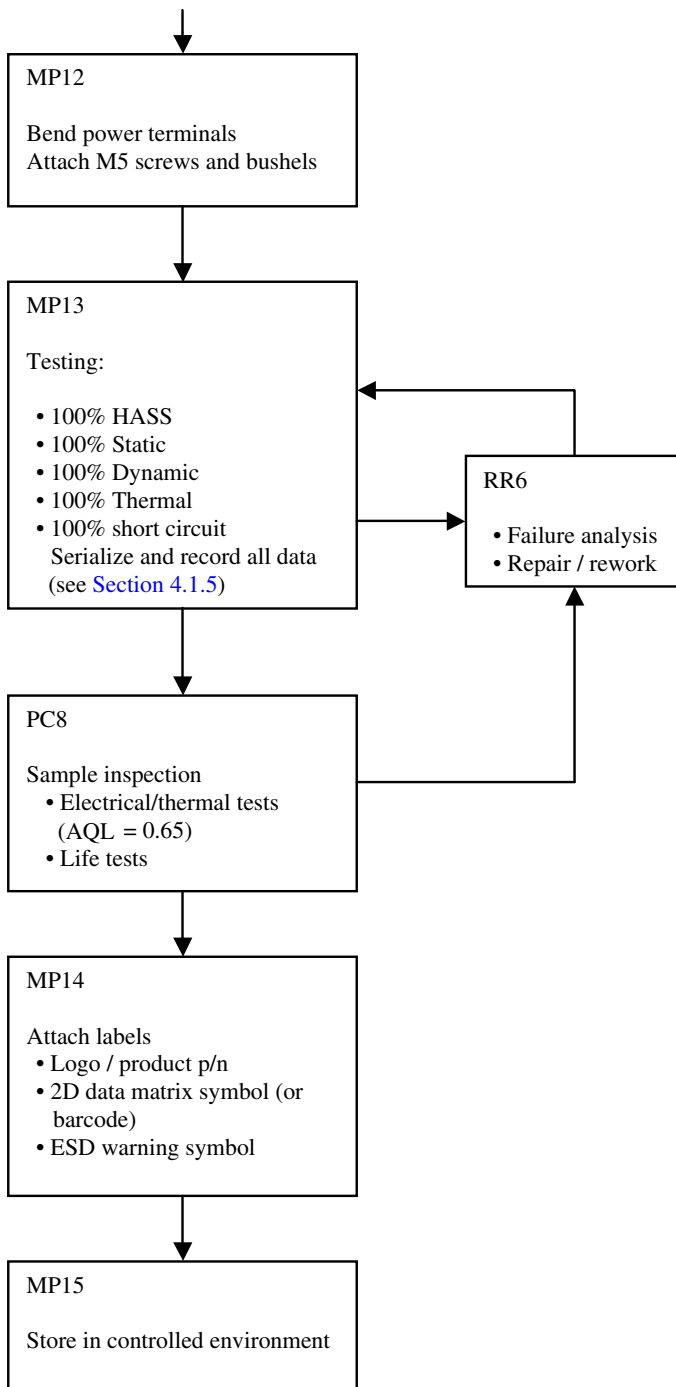


CHART 4.4D

This chapter focuses on the design of a power IGBT module. The vehicle for design is the popular 200-A, 1200-V, 1000-W, dual IGBT module in a half-bridge configuration, packaged in the industry standard Double Int-A-Pak. The schematic diagram and the pin-out assignment are shown in [Figure 5.1](#) and [Figure 5.2](#).

The design of the module is a three-step process. The IGBT module is a multilayered structure with different materials in intimate contact with each other. Thermal interactions between these materials play an important role in the long-term reliability of the product. The module must, therefore, be properly thermally managed. Once the thermally sound stack structure has been established, the next step is the physical layout of the module. This requires circuit partitioning and design guidelines.

- **Step 1: Thermal management** — Here, a preliminary stack structure is proposed based on the selected materials from [Chapter 3](#). Thermal analysis on conduction and stress are performed. The selections and the respective parameters are then adjusted repeatedly until the calculated T_j rise and the stress are within the desired levels, which are derived from the environmental and power dissipation requirements of the module.
- **Step 2: Circuit partitioning** — The circuit is partitioned into segments to optimize function, performance, reliability, and cost. Steps 1 and 2 are somewhat interdependent and can be undertaken concurrently.
- **Step 3: Design guidelines and considerations** — These include the following:
 - General guidelines for the materials:
 - Ceramic substrate
 - Metallization pattern on ceramic substrate
 - Metal baseplate
 - Terminals
 - Plastic case and cover

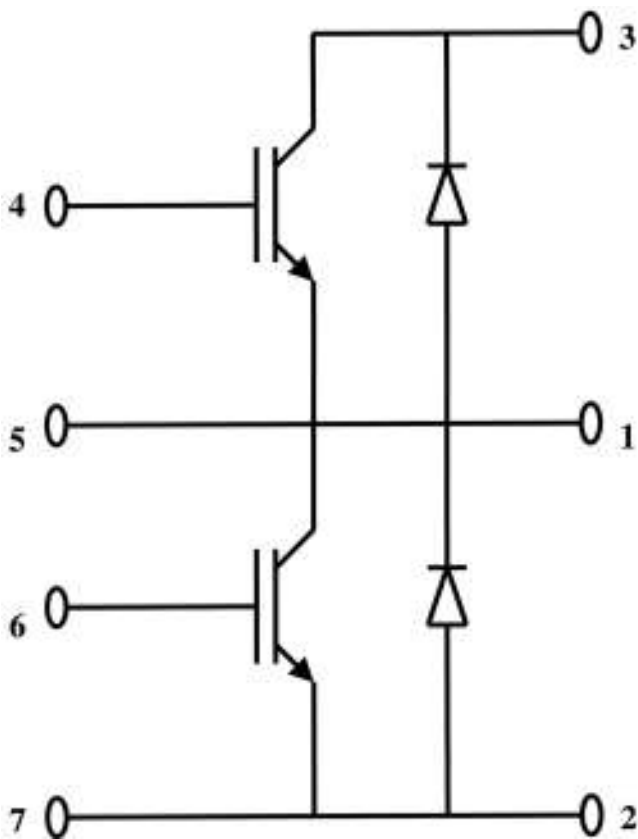


FIGURE 5.1
Half-bridge circuit configuration.

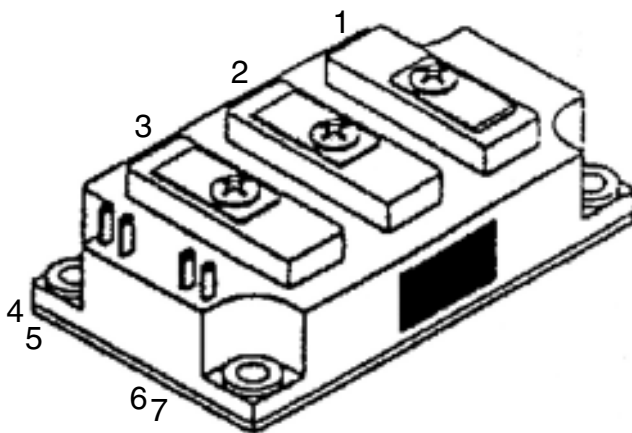


FIGURE 5.2
Double Int-A-Pak (isometric).

- Specific guidelines from the suppliers of the materials
- Assembly or design for manufacturing guidelines
 - Cleaning
 - Solder printing and dispensing
 - Wire bonding
 - In-line testing
- General industry standard guidelines
 - Mil-Std-883, 105
 - UL, VDE, CSA
 - IPC

There are numerous CAD software programs available in the industry that can provide in-depth analysis of the thermal–electric and thermal–mechanical behavior of the modules. The following list represents a few of these programs that can be used for [step 1](#):

- Flotherm by Flomerics, Inc.
- BETAsoft by Dynamic Soft Analysis, Inc.
- Coolit by Daat Research Corp.
- ICEPAK and PakSi by Fluent
- DesignSpace 8.1 By AnSys
- EFC by MAYA

Some companies, such as Fujitsu Interconnect Technologies, also offer thermal analysis service.

A CAD system that can be used with Windows for laying out the metalization pattern in [steps 2](#) and [3](#) is offered by HEM Data Corp.

5.1 Thermal Management

5.1.1 Stack Structures^{1,2} (Table 5.1)

5.1.2 Thermal Conduction Analysis

Thermal analysis on conduction^{1–8} and stress^{4,5} are performed on a proposed preliminary stack structure. Repeated iterations and adjustments are made until the calculated T_j rise and stress magnitude are within the desired levels. The stack structures shown in [Table 5.1](#) are the results of these iterations.

Based on the values of the parameters, the calculated thermal resistance (assuming only conduction loss) for each design option is shown in [Table 5.2](#).

TABLE 5.1

Stack Structure of the Four Design Options

	1	2	3	4 ^a
Chip/substrate combination	4 IGBT 4 FRED 4 Substrates	4 IGBT 4 FRED 4 Substrates	4 IGBT 4 FRED 4 Substrates	4 IGBT 4 FRED 1 Substrate
Insulating substrate	DBC ^b 8 mil Cu 10 mil Al ₂ O ₃ 8 mil Cu	ABC ^c 8 mil Cu 25 mil AlN 8 mil Cu	ABC 8 mil Cu 25 mil AlN 8 mil Cu	ABC 8 mil Cu 40 mil Si ₃ N ₄ 8 mil Cu
Metal base plate	Cu 120 mil	Cu 120 mil	AlSiC 120 mil	
IGBT chip	100 A	100 A 0.523" × 0.523" × 0.0075"	100 A	100 A
FRED chip	100 A	100 A 0.360" × 0.360" × 0.030"	100 A	100 A
Solder 1	95 Pb/5Sn 2 mil preform	95 Pb/5Sn 2 mil preform	95 Pb/5Sn 2 mil preform	95 Pb/5Sn 2 mil preform
Solder 2 ^d	96.5 Sn/3.5 Ag 3–5 mil paste	96.5 Sn/3.5 Ag 3–5 mil paste	96.5 Sn/3.5 Ag 3–5 mil paste	

^a Patent pending.^b DBC: Direct bonded copper.^c ABC: Active brazed copper.^d For the three-solder process, the third solder for the attachment of the terminals and bridges can be 63 Sn/37 Pb. This can be applied by dispensing or as preform. Avoid using Sn/Bi (42/58) alloy. It has a low melting point of 138°C and forms an unstable ternary phase with Pb, SnPbBi, which melts at 96°C.**TABLE 5.2** $R_{th}(j-c)$ of the Four Design Options and Other OEM Products

Design	Junction to Case Thermal Resistance $R_{th}(j-c)$ (°C/W)
1	0.138
2	0.113
3	0.140
4	0.102
Hitachi MBM200JS12AW	0.120
Eupec BSM200GB120DN2	0.090
IR GA200TD120U	0.125
IXYS VDI200-12S4	0.110

At 200 A and a power dissipation of 1000 W (or 500 W for each IGBT), the T_j junction temperature rise for each case is shown in Table 5.3.⁴⁻⁸

In addition, as the 200-A current passes laterally through the copper conductors on the ceramic substrate, heat will be generated due to resistive losses in the conductor. This temperature rise is calculated to be less than 1°C. The total ΔT_{jc} is shown in Table 5.4.

The junction temperature, T_j , of the semiconductor chip has a profound effect on its service lifetime. It must be maintained within the 150°C rating.

5.1.3 Thermal Stress Analysis

When a semiconductor chip is attached to a ceramic substrate, which is then mounted on a metal baseplate, a five-layer structure is formed, composed of the following elements:

- Semiconductor chip
- Solder 1
- Ceramic substrate
- Solder 2
- Metal baseplate

TABLE 5.3
 ΔT_{jc} of the Four Design Options

Design #	Junction Temperature Rise with Respect to Case ΔT_{jc} (°C)
1	69
2	56.5
3	70
4	51

TABLE 5.4
Total ΔT_{jc} of the Four Design Options

Design #	Junction Temperature Rise with Respect to Case ΔT_{jc} (°C)
1	70
2	57.5
3	71
4	52

For a structure of this type, excessive thermal stress is observed when the structure is cooled down from the solder reflow process, because the reflow temperature is greater than the operating temperature. During temperature cycling from -40 to 85°C , the maximum stress will therefore occur at the low end, or -40°C .

The brittle nature of the silicon chip plays an important role in the stress analysis of the preceding structure. In practice, there are critical forces or stresses for these materials,^{4,5} (Table 5.5) which, when exceeded, are likely to produce fracture.

Critical Stress for Different Materials

Material	Critical Stress (psi)
Silicon	5.36×10^4 (for a $3\text{ }\mu\text{m}$ flaw)
Al_2O_3	4.98×10^4
AlN	4.44×10^4
Si_3N_4	1.40×10^5

Since silicon is brittle, its critical stress is flaw dependent and, in this case, is obtained by assuming a surface flaw of $3\text{ }\mu\text{m}$. This flaw may be created during sawing, lapping, or grinding. On the other hand, because Al_2O_3 , AlN , and Si_3N_4 are ductile, the critical stress corresponds to their tensile strength, which is defined as the stress required to stretch the material to its breaking point.

During temperature cycling from -40 to 85°C , the stress at the IGBT and the insulating substrate is maximum at -40°C . The following discussion presents are the calculated maximum stress for the four design options.⁴

The calculation is based on discussion in Reference 4, where the maximum stress at the chip corners is given by

$$S_M = \frac{(TCE_s - TCE_D) \times (T_p - T_A) \times L \times G \times \tanh(\beta)}{\beta \times t_B} \tag{5.1}$$

$$\beta = \sqrt{\frac{G}{t_s} \left(\frac{1}{E_D t_D} + \frac{1}{E_s t_s} \right)}$$

where

- S_M = Maximum stress at the chip corners
- CTE_s = Coefficient of thermal expansion of the substrate
- CTE_D = Coefficient of thermal expansion of the chip

- T_p^* = Processing temperature in °C (solidification temperature of solder)
- T_A = Ambient temperature
- L = Maximum chip dimension
- G = Shear modulus of solder
- t_B = Solder thickness
- t_S = Substrate thickness
- E_D = Modulus of elasticity of the chip
- t_D = Chip thickness
- E_S = Modulus of elasticity of the substrate

Table 5.6 shows the calculated maximum stress at the IGBT chip and the ceramic substrate of each design option.

TABLE 5.6

Maximum Stress at IGBT and Substrate of the Four Design Options

Design #	Maximum Stress at IGBT (psi)	Maximum Stress at Substrate (psi)
1	3.87×10^4	2.60×10^4
2	5.36×10^4	4.44×10^4
3	1.89×10^4	9.75×10^3
4	5.97×10^2	

When compared with the preceding critical stresses, the probability of crack or fracture will limit the temperature cycling ability of each design option, as shown in Table 5.7.

TABLE 5.7

Comparison of Temperature Cycling Ability for a 3 μm IGBT Flow

Design #	Temperature Cycling Ability from -40 to 85°C
1	Good
2	Fair
3	Very good
4	Excellent

The critical stress, $S^{4,9,10}$ for brittle materials like silicon is given by

$$S = Y \frac{K}{\sqrt{a \pi}} \quad (5.2)$$

* T_p should be the stress onset temperature.⁹

where

- K = Fracture toughness of the material (MPa – m^{1/2})
- $2a$ = Length of flaw
- Y = 1.3 for edge flaw
= 1.4 for surface flaw
= 1.56 for embedded flaw

Material	K
Silicon	0.7 – 0.8

If the flaw on the silicon power chip is 0.5 mil (12 μm) instead of 3 μm, the critical stress for fracture decreases to

$\sim 2.7 \times 10^4 \text{ psi}$

The temperature cycling ability of each design options becomes one of those shown in Table 5.8.

TABLE 5.8
Comparison of Temperature Cycling Ability for a 12 μm IGBT Flow

Design #	Temperature Cycling Ability from –40 to 85°C
1	Fair
2	Poor
3	Good
4	Excellent

A simplistic approach has been taken here in order to illustrate the effects of different parameters on thermal stress and temperature cycling. A more accurate prediction of temperature cycling capability must involve the fatigue properties of solder. The differences in the thermal expansion of the components during cycling will create a stress condition for the adjoining solder, which will eventually lead to creep deformation and stress relaxation. These inelastic properties of solder have already been incorporated into a well-developed, two-dimensional model, which can be used to provide detailed analysis of the following:¹⁰

- Stress magnitude and distribution
- Solder joint reliability and life

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5.2 Circuit Partitioning

A 200 A IGBT dual module in a half-bridge configuration has two identical sections in series. Each section has one 200 A IGBT chip and one 200 A FRED chip. Each of these 200 A chips can be made up of the following combinations:

- $1 \times 200 \text{ A}$
- $2 \times 100 \text{ A}$
- $4 \times 50 \text{ A}$

The first issue in designing this module is to determine which combination to use. In order to make the right choice, the following factors should be considered:

- Thermal stress between the chips and the insulating substrate
- Size of the insulating substrate
- Paralleling of IGBT chips
- Cost:
 - Chip
 - Labor (assembly, sorting)

5.2.1 Thermal Stress between the Chips and the Insulating Substrate^{1,2}

The brittle nature of silicon material results in a critical stress that can fracture the chip. This critical stress is surface-flaw dependent. For instance, a flaw

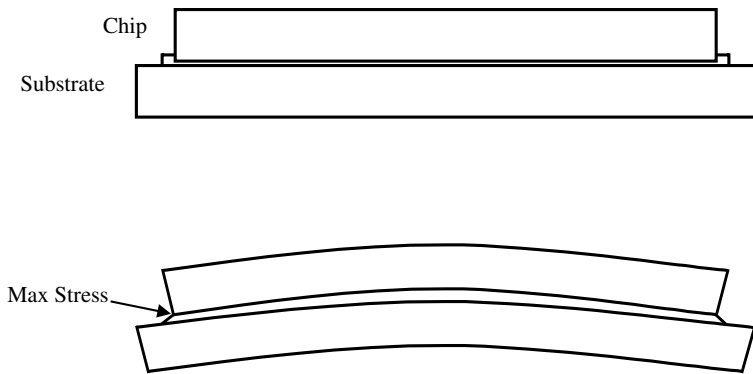


FIGURE 5.3
IGBT stack structure under stress.

of $3\text{ }\mu\text{m}$ yields a critical stress of about 5.3×10^4 . When the stress on the chip due to the TCE mismatch with the substrate exceeds this figure, fracture is likely.

The stress on the stack is illustrated in Figure 5.3.

The thermal stress that is exerted on the power chip (IGBT, FRED) is a function of the following:

- TCE mismatch between the power chip and the insulating substrate
- Insulating substrate material and thickness
- Power chip size and thickness
- Solder processing temperature
- Solder elastic modulus
- Solder thickness

Due to the TCE mismatch, the larger the chip size, the higher will be the thermal stress exerted on the chip. There is, therefore, a maximum chip size that a particular substrate can accept. The following two cases show the calculated maximum thermal stress vs. chip size for two popular solder alloys and the three selected insulating substrates: 96% Al_2O_3 , AlN , Si_3N_4 . At the same current rating, *the IGBT chip is larger than the FRED chip*. Therefore, the focus here is on the IGBT chips only, although the same conclusions apply to FRED chips.

- Power chip thickness: 0.015"
- Insulating substrate thickness: 0.050"
- Solder alloy preform thickness: 0.002"
- Ambient temperature: -40°C (At this temperature, the thermal stress on the chip is highest.)

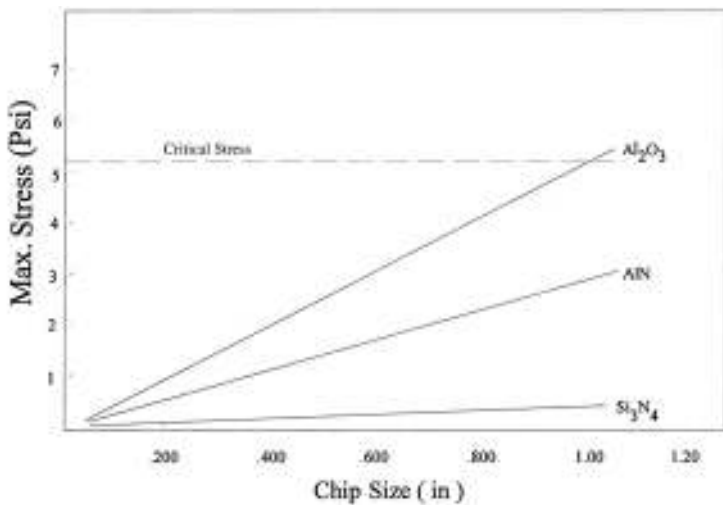


FIGURE 5.4

Calculated maximum stress vs. chip size for 96.5Sn3.5Ag solder.

The following results are obtained by applying Equation 5.1.

5.2.1.1 Case 1

Solder alloy: 96.5Sn3.5Ag. See Figure 5.4.

5.2.1.2 Case 2

Solder alloy: 95 Pb5Sn. See Figure 5.5.

The results are summarized in Table 5.9.

5.2.2 Size of Insulating Substrate

The size of the insulating substrate for a 200-A IGBT dual module can be estimated by adding the areas required for the following:

- Total IGBT chips in a dual module (8×50 A, 4×100 A, or 2×200 A)
- Total FRED chips in a dual module (4×100 A or 2×200 A)
- Cu metallization area for three terminals
- Cu metallization area for Al wire bonding
- Cu metallization area for conduction

This is estimated to be about 6 in², or 2" $\times$ 3".

Without any elaborate and expansive lapping, standard warpage for insulating substrates Al₂O₃ (96%), AlN, and Si₃N₄ is

3 to 3.5 mils/1"

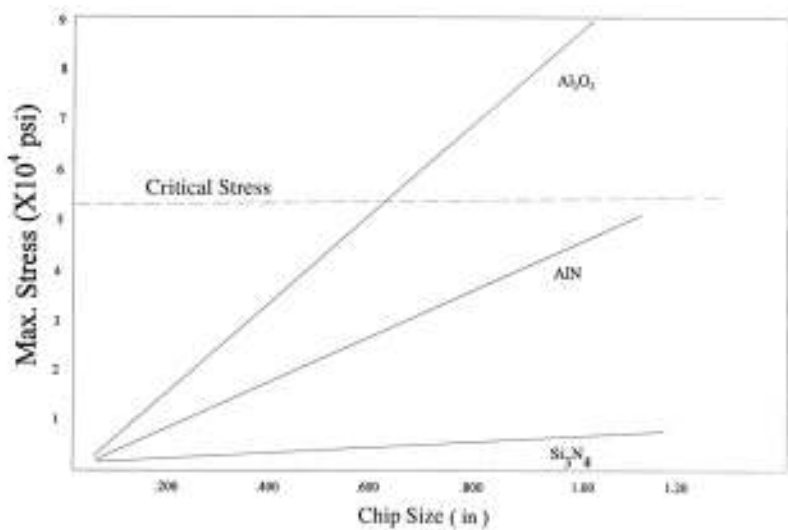


FIGURE 5.5
Calculated maximum stress vs. chip size for 95Pb5Sn solder.

TABLE 5.9

Allowable Maximum Chip Size for Different Insulating Substrates

	Allowable Maximum Chip Size	Based on IXYS, IR, APT, IGBT Chip Specifications
<i>Case 1. Solder alloy: 95Pb5Sn</i>		
Al ₂ O ₃	1" × 1"	Can accept 200 A chip
AlN	> 1" × 1"	Can accept 200 A chip
Si ₃ N ₄	> 1" × 1"	Can accept 200 A chip
<i>Case 2. Solder alloy: 95Pb5Sn</i>		
Al ₂ O ₃	0.6" × 0.6"	Can accept 100 A chip
AlN	> 1" × 1"	Can accept 200 A chip
Si ₃ N ₄	> 1" × 1"	Can accept 200 A chip

A 2" × 3" substrate can therefore have a warpage of almost 10 mils from center to end. Considering that the solder paste thickness is only about 3 to 5 mils, this warpage is not acceptable. A more feasible approach is to divide the substrate into either two small substrates at 2" × 1.5" each or four smaller substrates at 1" × 1.5" each. The four-substrate combination is preferred because this yields a more manageable warpage. These four substrates are actually two identical pairs. Each small substrate will then carry either a 1 × 100-A or 2 × 50-A IGBT chip and a 1 × 100-A FRED chip. *The completed*

small substrate is treated as an independent unit, sample or 100% tested, sorted, and inspected before committing to full module assembly.

For stand-alone, one-piece Si_3N_4 substrate, the top/bottom Cu metallization must be optimized to produce a positive convexity specification. Here, a $1 \times 200\text{-A}$ IGBT chip can be used.

5.2.3 Paralleling of IGBT Chips^{3,4}

When paralleling IGBT chips, the first issue is how well they share the total current. This will eventually lead to how closely matched they are in junction temperature (T_j) and whether or not one of the chips approaches the rated T_j . *Because T_j directly correlates to reliability, this is the primary concern.*

Two factors should be considered in paralleling IGBTs: electrical matching and thermal coupling.

5.2.3.1 Electrical Matching^{3,4}

Electrical matching is an effective way to parallel IGBT chips. The matching criterion is based on measuring the forward voltage drop across the IGBT in a diode mode configuration, V_{CESAT} (on). For current sharing to be within $\pm 15\%$,

$$V_{\text{CESAT}} \leq 0.30 \text{ V.}$$

Grouping four 50-A IGBT chips to within 0.30 V is more difficult and time consuming than grouping two 100-A chips.

5.2.3.2 Thermal Coupling³

If current sharing were not perfect, a good thermal coupling between paralleled IGBT chips would help reduce the thermal imbalance. Thermal coupling depends on the following:

- Solder attachment between the chips and the insulating substrate
- Thermal conductivity of the insulating substrate
- Solder attachment between the insulating substrate and the metal base plate
- Thermal conductivity of the metal base plate

5.2.4 Cost

- **Chip** — As chip size increases, the cost increases faster than the area ratio due to the fact that both the wafer testing yield and the number of available chips on a wafer decrease nonlinearly with chip size.

Hence, the cost of a 200-A chip is more than quadruple (5.5×) and the cost of a 100-A chip is more than double (2.5×) the cost of a 50-A chip.

- **Labor:**
 - Assembly — Here, the labor cost is lowest for the 1 × 200-A and highest for the 4 × 50-A combination, with the 1 × 100-A in between.
 - Sorting — Sorting labor involved in grouping four 50-A IGBT chips is much higher than for two 100-A chips.

Taking into account all the preceding mechanical, electrical, thermal, and economic considerations, it appears that the combinations shown in Table 5.10 are appropriate for the 200-A, 1200-V IGBT dual module.

TABLE 5.10
IGBT/FRED Chip and Substrate Combination for Different Insulating Substrates

Insulating Substrate	IGBT/FRED Chip and Substrate Combination
Al ₂ O ₃	4 small substrates Per substrate: 1 × 100-A IGBT; 1 × 100-A FRED
AlN	4 small substrates Per substrate: 1 × 100-A IGBT; 1 × 100-A FRED
Si ₃ N ₄	1 whole-piece substrate Either a 100-A or a 200-A chip is acceptable

References

1. Sergeant, J.E. and Krum, A., *Thermal Management Handbook for Electronic Assemblies*, McGraw-Hill, New York, 1998.
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5.3 Design Guidelines and Considerations

This section contains general guidelines. Because each supplier has its own specific design rules, these must be reviewed before any physical layout is done.

TABLE 5.11**General Design Guidelines for Ceramic Substrate**

Length and width	4" × 4" maximum ± 0.8% tolerance
Thickness	8–80 mil 25 mil standard ± 8% tolerance Stamping < 40 mils Dry-press > 40 mils
Warpage (or camber)	3–3.5 mil/inch
Surface roughness	Ra ≤ 0.7 μm Rz ≤ 3.5 μm
Holes	Diameter ≥ 0.060" ± 0.004" Distance from edge ≥ 0.060"
Burrs	≤ 2 mil
Blisters	≤ 1 mil
Cracks	< 20 mil from the edges
Radius of curvatures/corners	0.080" (typ.)
Parallel between surfaces	± 0.04% of outside dimensions
Perpendicularity	± 0.04% of outside dimensions

TABLE 5.12**General Properties of Ceramic Substrate**

	Al ₂ O ₃	AlN	Si ₃ N ₄
Thermal conductivity (w/mk)	24	170	70
CTE (ppm/°C)	6	4.6	3
Dielectric strength (V/mil)	300	375	250

5.3.1 Ceramic Substrate¹

The general design guidelines and properties of ceramic substrate are shown in Table 5.11 and Table 5.12.

5.3.2 Metallization Pattern on the Ceramic Substrate

The pattern layout is based on the following guidelines and specifications.^{1–5}

5.3.2.1 Dimensions

The dimension and pin-out assignment should be consistent with the industry's standard 200-A 1200-V half-bridge IGBT module specifications.

- Hitachi — MBM200JS12AW
- Eupec — BSM200GB120DN2
- Powerex — CM200DU-24F
- IR — GA200TD120U
- IXYS — VDI200-12S4

5.3.2.2 Guidelines for DBC- Al_2O_3 , ABC-AlN, Si_3N_4 Metallization Pattern

Table 5.13 presents the guidelines for direct bonded and active brazed copper metallization on ceramic substrate.

The voltage overshoot from stray inductance, L , is given by

$$V = L \, di/dt \quad (5.3)$$

where di/dt = turn-off di/dt .

In a typical IGBT power switching circuit,

$$di/dt \sim 0.01 \times I_C \, A/\mu s. \quad (5.4)$$

At 200 A, $di/dt \sim 2A/\mu s$. For $L = 50 \, nH$, $V = 100 \, V$.

Stray inductance must be kept to an absolute minimum. The layout should be tight, compact, and as symmetrical as possible. The conducting path should be short and wide. The stray inductance, L , can be estimated from the following equations:

Flat:

$$L \sim 5 \left\{ \ln 2 \, l / (w + t) + \frac{1}{2} + 2 / 9 \frac{w + t}{1} \right\} nH / in \quad (5.5)$$

where l , w , t are the length, width, and thickness, respectively, of the conductor.

Round:

$$\sim 51 \ln \frac{4l}{d} \, nH / in \quad (5.6)$$

where d is the diameter.

TABLE 5.13Design Guidelines for DBC- Al_2O_3 , ABC- AlN , Si_3N_4 Metallization Pattern

Thickness of Cu (not to exceed the ceramic thickness)	6–20 mil (10 mil typ.) 8–12 mil (10 mil typ.)	Direct-bonded Cu Active-brazed Cu
Tolerance for thickness	$\pm 10\%$	
Minimum line width	20 mil 40 mil	6–10 mil Cu 10–20 mil Cu
Tolerance for length and width	± 4 mil	
Minimum separation between conductors	20 mil 40 mil	< 12 mil Cu 12–20 mil Cu
Etch factors, a	3–10	Undercutting = $\frac{\text{thickness}}{a}$
Minimum distance from substrate edge	20 mil	$V_{\text{ISO}} = 2,500 \text{ V}$
Camber	$\pm (3\text{--}4 \text{ mil/linear inch})$	
Hole	Hole $\geq$ substrate thickness Edge of hole $\geq 0.060''$ from edge of substrate	
Cu conductor sheet resistivity	0.00017 $\Omega/\text{sq.}$ 0.00006 $\Omega/\text{sq.}$	4-mil thick Cu 12-mil thick Cu
Acceptable temperature rise of conductor under rated steady-state condition	10–20°C	
Minimum isolation voltage between conductor pads on top side	1,500 V_{AC} for 1 min	
Minimum isolation voltage between top and bottom conductors (UL1550)	2,500 V_{AC} for 1 min	
Rounded corners between high-voltage pads Radius of curvature	20–60 mil typ.	
Total stray inductance (metallization, terminals, aluminum wires, and bridges)	< 50 nH 20 nH (typ.)	

(continued)

TABLE 5.13 (continued)**Design Guidelines for DBC-Al₂O₃, ABC-AlN,Si₃N₄ Metallization Pattern**

Top-side Cu/bottom-side Cu		
Thickness ratio	1–1.5	
Coverage ratio	0.75–1	
Metallization edge	Step or dimple shape for stress relief; step height or dimple depth should be about half of Cu metallization thickness	
Area for chip attachment	A minimum of 20 mils beyond the chip dimensions on all sides	
Area for terminal attachment	A minimum of 20 mils beyond the foot dimension on all sides	
Area for aluminum-wire bond	3 × 5 the diameter of aluminum wire ⁶	
Minimum substrate wire bond sites from the edge of the chip	40–60 mils	
Maximum aluminum-wire length	300–500 mils	
Wire-bonding from chip to chip is not recommended		
All wire bonds must terminate on the ceramic substrate		
Wires crossing over is not permitted (Mil-883C)		
Height difference between first and second bond	30 mils maximum	
Area for in-process production testing	20 × 20 mils area on the gate, emitter, and collector patterns; 40-mil minimum distance from the chips and the nearest wire	
Minimum distance between components	40 mils Aqueous cleaning is not effective for tight spacing	
To reduce any thermal crosstalk, chips on the same ceramic substrate should be separated by a minimum distance of D/2, where D = dimension of the larger chip		
Cu peel strength	> 150 N/cm	Push–pull gauge test
Cu surface — Discolored section, stain	Not allowed	
Burrs, protrusion	1 mil max critical area 4 mils max free area	
Pits, voids	Not allowed critical area 80 mil, Cu thickness-free area	
Crack	Not allowed	

Due to the voltage overshoot, the IGBT and FRED should be derated to 80 to 85% of the voltage ratings.

For Si_3N_4 substrate with no base plate, the type and magnitude of the warpage facing the heat sink must be optimized. A positive convexity of about 1 mil/1" is desirable. The key controlling factors are as follows:

- The thickness of the Si_3N_4 substrate
- The ratio of thickness and coverage of top-to-bottom Cu metallization (Some OEM suppliers prefer a prebent ceramic substrate⁵.)
- The consistency of the same surface for the top or bottom metallization

In general, the thinner the substrate, the higher the ratio and the larger the warpage will be. Excessive warpage, however, may create cracks during screw mount down.

The other parameter that should be considered is the surface roughness, which has a direct impact on the thermal conductance between the substrate and the heat sink. This should be controlled to about 1 μm .

Zirconia-reinforced Al_2O_3 ceramic (10 to 15% ZrO_2) is an alternative to Si_3N_4 for this baseplate design. It is mechanically strong and much lower in cost. The drawback is its low thermal conductivity: about one third that of Si_3N_4 .

An example of a DBC metallization layout on a 25-mil Al_2O_3 substrate is shown in [Figure 5.6](#).

5.3.2.3 *Plating*

The general guidelines for Ni plating are presented in [Table 5.14](#).

5.3.3 Metal Baseplate

5.3.3.1 *Dimensions*

The dimensions of the baseplate should be consistent with those of the industry standard, Double Int-A-Pak.

- Baseplate: $2.44" \times 4.25" \times 0.118"$
- Tolerance for length/width: $\pm (0.2 \text{ to } 0.5)\%$
- Thickness: $\pm (2 \text{ to } 3)\%$

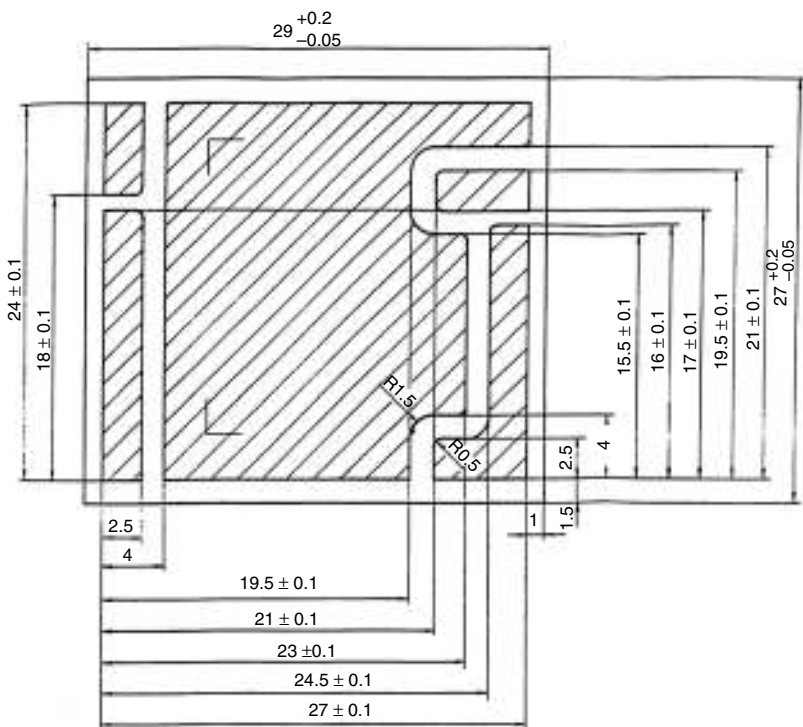


FIGURE 5.6

A DBC metallization pattern on a 25-mil Al_2O_3 substrate (24 mm $\times$ 29 mm).

TABLE 5.14

Guidelines for Ni Plating

Electroless Ni/P Plating	P content 8–12%
Thickness	2–5 μm
Adhesive-tape test	10 sec
Pull-test strength	2.5 N (or 300 gm) min
for 12-mil Al wire	5–6 N (600–700 gm) typ.
Solderable for Sn/Pb and Su/Ag/Cu	Solders wetting $\geq 95\%$
	260°C for 10 s
Surface roughness	15 μm maximum
Blisters, stains, discoloration,	Not allowed
peel-off, scratches	410°C for 5 min — no blister
Alignment marks for chips and to baseplate	
These should be nonsymmetrical for orientation and identification	

5.3.3.2 Baseplate Characteristics

- Cu baseplate should be prebent in a concave upward or positive convex manner toward the heat sink to compensate for the warpage created during solder reflow.^{3,7} The finished module should have an upward concavity. *A perfectly flat surface is not preferred.*
 - Concavity from center to short edge: 5 mils (typ.)
 - Concavity from center to long edge: 3 mils (typ.)
- AlSiC baseplate should also be prebent, perhaps to a lesser degree than copper, due to its lower CTE.
- Another possibility is one side bow, with one surface flat and the other convex. The ceramic substrate is attached to the flat side, and the convex side faces the heat sink.
- All corners should be rounded — Rounded radius of curvature: 0.1" typ.
- Hole — Hole diameter/baseplate thickness ≥ 1 :
 - Edge of hole must be 0.060" minimum from edge of baseplate.
 - Edge of hole must be free of burrs and ridges.
- Defects:
 - See Table 5.15
- Plating:
 - Electroless Ni/P plating, phosphorous content 8 to 12% (Mil-C-26074, class I, Grade A) or Cr/Ni/Ti plating.
 - Solderable with Pb/Sn and Sn/Ag/Cu solders; wetting $\geq 95\%$; tape test 10 sec.
 - Thickness $\sim 5\ \mu\text{m}$.
 - Smooth and uniform appearance.
 - Blisters, stains, discoloration, and peel-off not allowed.
 - Alignment marks for ceramic substrate alignment should be on the top concave surface. These marks should be nonsymmetrical to ensure proper orientation.

An example of copper plate is shown in [Figure 5.7](#).

TABLE 5.15

Maximum Allowable Defects

Burrs and protrusions:	1.0 mil height, 10 mil length max
Pits, dents, voids	2 mil deep and 5 mil diameter max
Scratches, grooves	2 mil deep, 10 mil length max
Cracks	Not allowed
Maximum allowed defects	3 per square inch in critical area

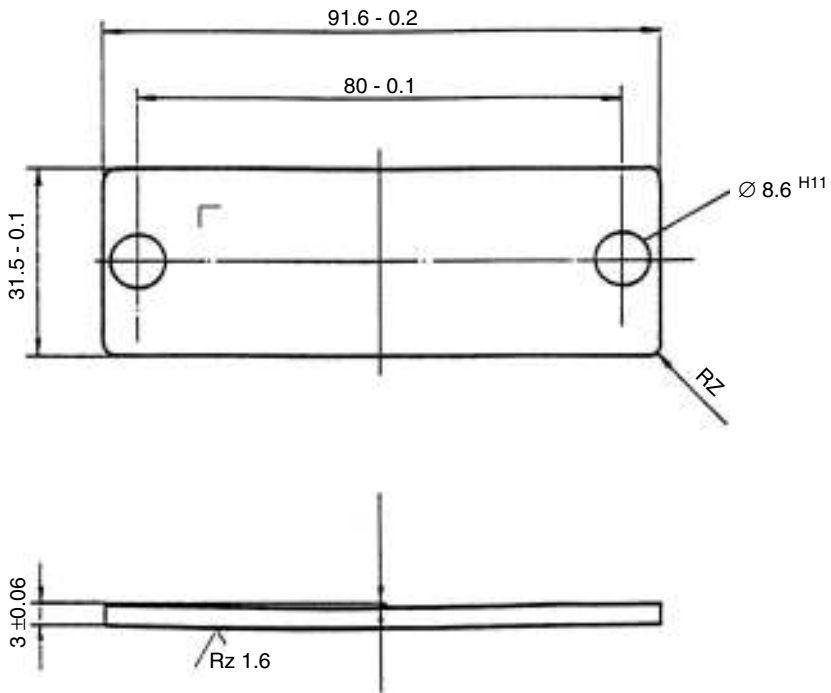


FIGURE 5.7
A Cu baseplate (31.5 μm × 91.6 μm).

5.3.4 Power Terminals/Fast-On Tabs/Connecting Bridges

5.3.4.1 Dimensions

The dimensions should be consistent with those of the industry standard, Double Int-A-Pak.

5.3.4.2 Materials

Materials used can be of the following:

- Beryllium/Copper (C170, C172)
- Beryllium/Nickel (Ni200, Ni270)
- Pure Cu OFHC half hard

5.3.4.3 Power Terminals

- Voltage drop across terminals at rated current:
 - < 0.05 V/terminal
 - Temperature rise: < 20°C

- Terminals should be able to accommodate 0.250" diameter holes for M5 screws.
- Terminals can be etched or stamped from Cu, Cu/Be, or Ni/Be sheet.
- Dimensions and tolerances are shown in Table 5.16.
- Terminals should have notches (~ one-half thickness, 0.040" length) for bending above the lid and holes for anchoring in epoxy resin.
- Terminal foot should be multipronged and bent to provide multiple soldering contacts and stress relief.
- The stray inductance must be kept at an absolute minimum. The terminal foot should be soldered near the IGBT chips. Because the terminal length (or height) is fixed, the width and thickness should be made as large as practically possible (use Equation 5.5). For the half-circular bent, double the contribution of the regular length.
- Dimensions:
 - $L \sim 1.80$ to 2.00 "
 - $W \sim 0.70$ to 0.90 "
 - $d \sim 0.045$ – to 0.055 "
- Screw ratings:
 - M3 — 60 A continuous
 - M5 — 200 A continuous
 - M6 — 400 A continuous

TABLE 5.16

Dimensions and Tolerances for Power Terminals

Holes (or slots)	
Metal thickness	Diameter (or width)
1–5 mils	$\geq$ metal thickness
> 5 mils	$\geq 1.1 \times$ metal thickness
Finger-width	
Metal thickness	Width (or distance between holes)
≤ 5 mils	$\geq$ metal thickness
> 5 mils	$\geq 1.25 \times$ metal thickness
Length/width/thickness tolerances	
Length/width	Tolerance
< 1 "	± 0.0005 "
1–3"	± 0.001 "
3–6"	± 0.002 "
Thickness	Tolerance
0.010"	± 0.0015 "
0.020"	± 0.0030 "
0.040"	± 0.0050 "

Bent radius: For 1/2H BeCu, minimum bent radius $\sim$ metal thickness.

- The materials for the screws and terminals should be close together in the galvanic series of metals:

Mg	Pb	Bronze
Zn	Sn	Cu/Ni alloys
Al	Ni	Ag
Cr	Brass	Au
Steel	Cu	Pt

- Defects
 - Burrs and protrusions — 2 mil max
 - Nicks, scratches, grooves, dents, sharp corners — Not allowed

5.3.4.4 *Fast-On Tabs*

- Industry standard size: 0.110" W × 0.020" thick
- The tabs are anchored either in the case or in the lid. The lower halves are embedded in the epoxy resin, which provides further mechanical support. Tabs must withstand 25 repeated insertions and withdrawals at 4.5-Kg force.
- Fast-on tab rating:
 - 0.110" (2.8 μm) 20 A continuous
 - 0.192" (4.8 μm) 40 A continuous
 - 0.250" (6.3 μm) 60 A continuous
- Insulating wires for tabs:
 - Temperature rating for the insulation should be, for example , EE, class F for a maximum operating range of 155–179°C or class H for 180–199°C.
 - Use 500 circular mils per ampere to determine AWG.
 - Use stranded wire for better stress relief.

TABLE 5.17
AWG vs. Current Carrying Capability

AWG	I (A)
14	8.22
16	5.16
18	3.24
20	2.04
22	1.28

- Use the minimum length required to reduce stray inductance, but keep it loose enough to avoid any breakage from stress or mishandling. Use Equation 5.6 to calculate the stray inductance.
- Use different colors to distinguish between gate and emitter.
- Twist the gate and emitter wires of each IGBT.
- Avoid bundling together the wires from different IGBTs.
- Defects
 - Burrs and protrusions — 2 mil maximum
 - Nicks, scratches, grooves, dents, sharp corners — Not allowed

5.3.4.5 *Plating*

The most common used plating is electroless Ni/P plating, with P content 8–12% (Mil-C-26074, Class I, Grade A)

- Thickness — $\sim 5\ \mu\text{m}$
- Blisters, stains, discoloration, peel-off — Not allowed

5.3.4.6 *Connecting Bridge*

Connecting the substrates can be accomplished by wire bonding or by Ni-plated Cu stripes, which are usually bent half circular for stress relief.

Examples of power terminal, fast-on tabs, and connecting bridge are shown in [Figure 5.8](#), [Figure 5.9](#), and [Figure 5.10](#), respectively.

5.3.5 *Plastic Case and Cover*^{2,8}

- Consistent with dimensions of the industry standard, Double Int-A-Pak
- Suggested Material — DAP or PBT (with glass fiber as filler)
- Color — Black
- Wall thickness — 0.050 to 0.070"
- Thickness tolerance:
 - $\pm 0.005''$ — Below 0.5" high
 - $\pm 0.010''$ — From 0.5 to 1.0" high
 - $\pm 0.015''$ — Higher than 1.0"
- Length, width, height tolerances:
 - $\pm 0.010''$ — Under 1"
 - $\pm 0.015''$ — Between 1 and 3"
 - $\pm 0.020''$ — Above 3"

- External radius of curvature — ± 0.015 " maximum
- Internal radius of curvature — $1/64$ to $1/16$ ", depending on size ($1/16$ " for $3" \times 4"$ case)
- Dimension of overhang lip:
 - 0.035 " — Thick (typ.)
 - 0.050 " — Overhang (typ.)
- Burr — ≤ 2 mils
- The cover and the case are attached by epoxy, usually in the form of B-staged film. The cover can also snap on to the case mechanically.
- The cover can have deep grooves or tall partitions between terminals to provide the necessary creepage distance, which is 16 mm for 1000 V, as specified by UL508 and VDE0160 standards.
- The cover should have three pockets to provide space for the three M5 screws. Each pocket should have a hexagonal compartment for the nut.
- The cover should have openings, such as grooves, to provide easy access for pouring or dispensing silicone gel and epoxy resin.

5.3.6 Solder Preform

- Available for both Pb and Pb-free solder
- With or without flux
- Length, width tolerance:
 - ± 0.001 " — 0.010 to 0.060 "
 - ± 0.002 " — > 0.060 "
- Thickness tolerance:
 - ± 0.0002 " — 0.001 to 0.002 "
 - ± 0.0004 " — 0.002 to 0.010 "
 - ± 0.001 " — 0.010 to 0.020 "
 - ± 0.002 " — > 0.020 "
- Allow 0.003 " on each side for solder spread during reflow.

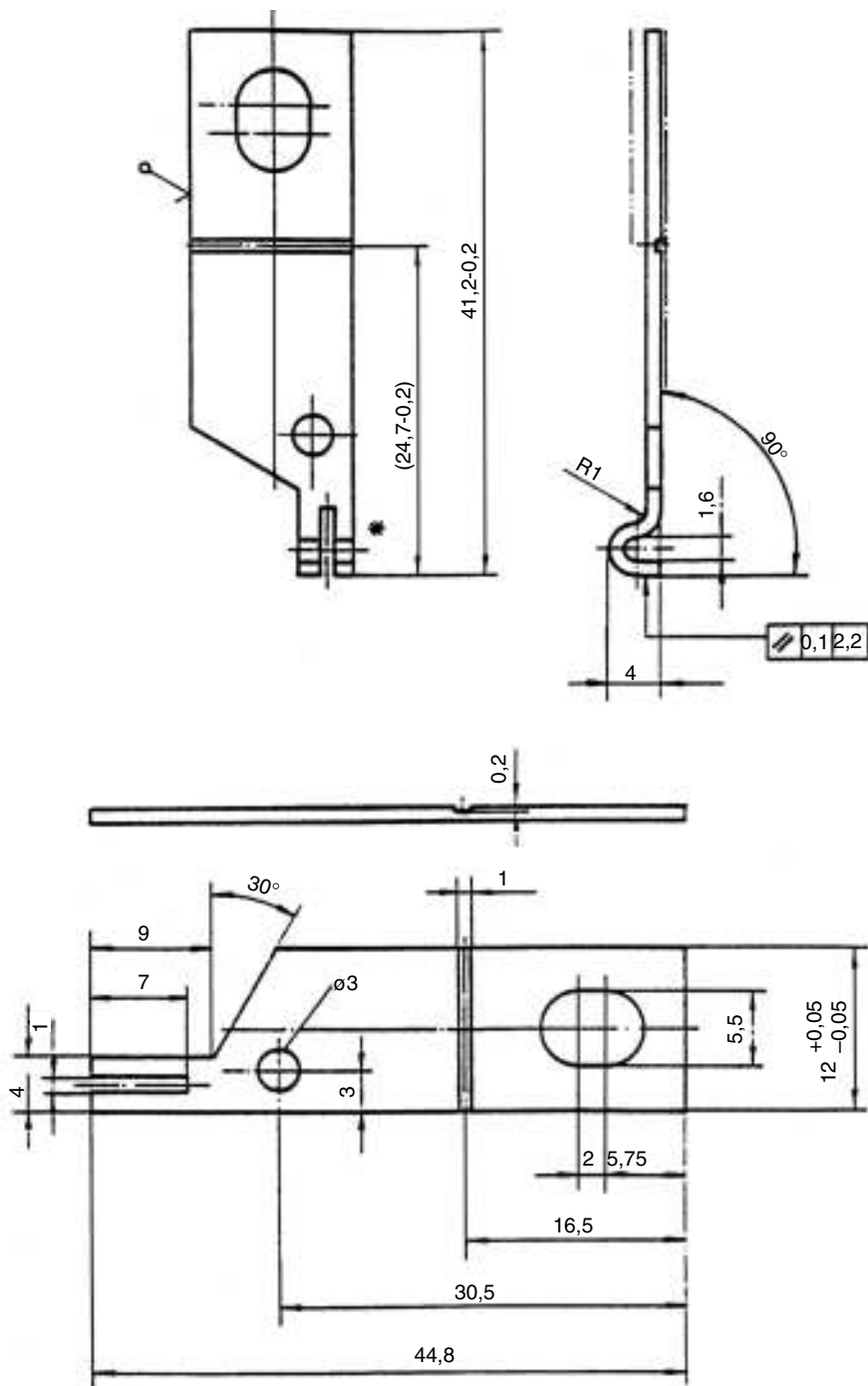


FIGURE 5.8
Power terminal (12 mm × 45 mm).

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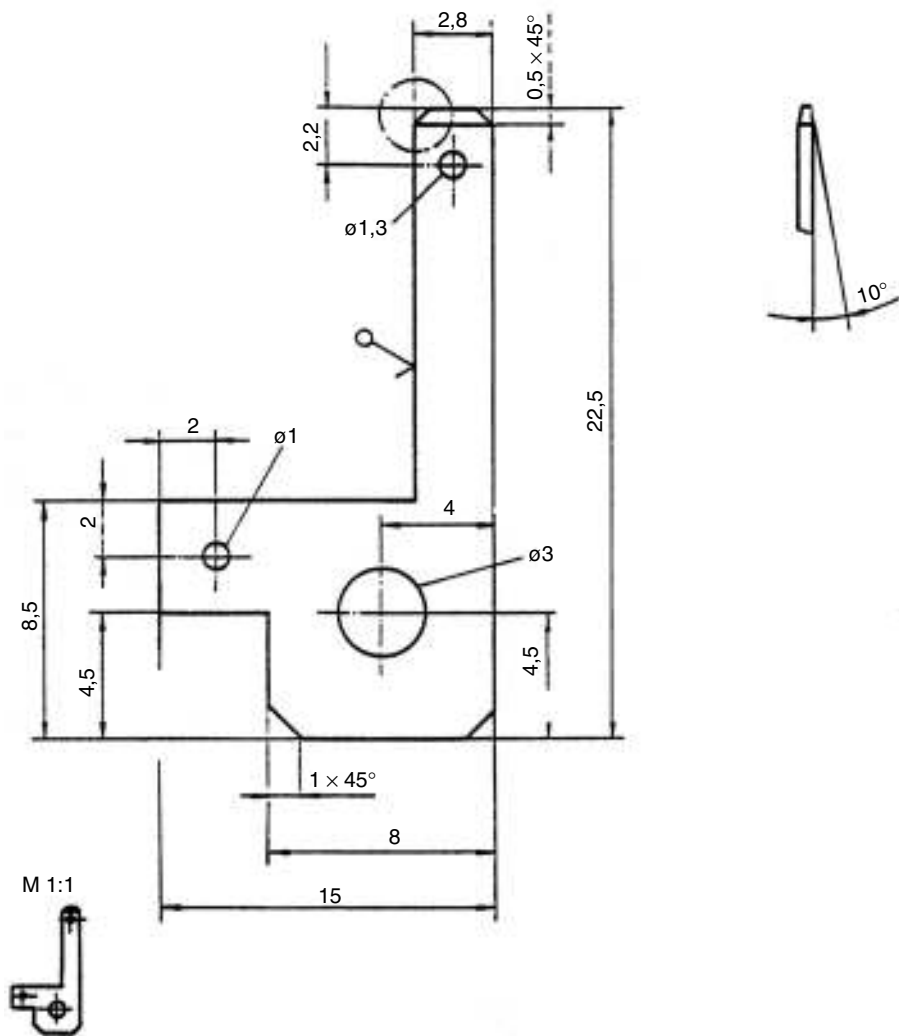


FIGURE 5.9
Fast-On tab (2.8 mm x 22.5 mm).

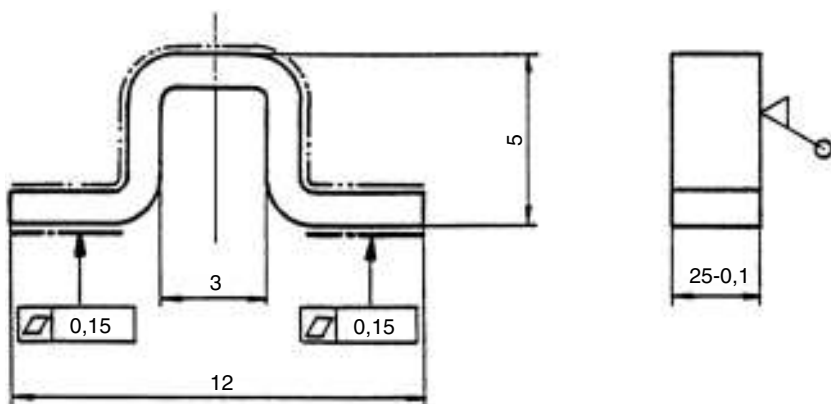


FIGURE 5.10
Connecting bridge (2.5 mm × 12 mm).

References

1. Denka Technical Information, *Standard Design Rules of Denka AN Plate*, No. ANB/CC/1/001, 1998.
2. Harper, C.A., *Electronic Packaging and Interconnection Handbook*, 2nd edition, McGraw-Hill, New York, 1997.
3. Licari, J.J. and Enlow, L.R., *Hybrid Microcircuit Technology Handbook*, Noyes Publishing, Park Ridge, NJ, 1998.
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5. Curamik Electronics, GmbH, *Direct Copper Bonded Substrates for Semiconductor Power Devices*, Curamik Report, 1997.
6. Orthodyne Electronics, Inc., *Design Guidelines*, Orthodyne Technical Pub., 2000.
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8. Robison Electronics, Inc., *Tolerance and Materials: Diallyl Phthalate Properties*, 2000.

5.4 Samples

Four groups of samples have been built according to the stack structures outlined in [Section 5.1.1](#). These samples are assembled based on the processes and the manufacturing flow charts outlined in [Chapter 4](#). Thermal mechanical and thermal impedance (or heating) characterization of these samples are measured, and the results are presented in [Section 5.4.3](#).

TABLE 5.18

Estimated Manufacturing Cost of the Four Design Options

Design #	Estimated Manufacturing Cost ^a 200-A Dual IGBT Module (US\$)
1	60
2	75
3	85
4	65

^a This cost is based on offshore assembly in China and standard electrical testing. According to the U.S. Bureau of Labor Statistics, the hourly labor rate in China is \$0.40 vs. \$20.32 in the U.S. and \$2.34 in Mexico.

5.4.1 Estimated Manufacturing Cost

Table 5.18 shows the estimated cost, including both material and assembly labor, for each design option of the 200-A, 1200-V dual IGBT module in a half-bridge configuration.

5.4.2 Theoretical Comparison of Design Option

Table 5.19 presents a theoretical comparison of the different design options based on calculation from [Sections 5.1.2](#) and [5.1.3](#).

5.4.3 Thermal Behavior of the Samples

5.4.3.1 Thermal Mechanical Characterization¹

The type, magnitude, and distribution of the deformation or warpage across the entire power chip (IGBT, FRED) and baseplate are measured nondestructively.

TABLE 5.19

Theoretical Comparison of the Four Design Options

	1	2	3	4	Hitachi ^a
Thermal resistance (C/W steady state)	0.138	0.113	0.140	0.102	0.120
Thermal fatigue capability (−40 to 85°C)	Good	Fair	Very good	Excellent	Good
Approximate weight	400	400	300	250	450
Estimated manufacturing cost (US\$)	60	75	85	65	100 ^b

^a P/N: MBM200JS12AW.

^b Sales price at a quantity of 1000 pieces.

TABLE 5.20

Structure of the Four Sample Groups

Samples	1	2	3 (A, B)	4
Chip	IGBT/FRED	IGBT/FRED	IGBT/FRED	IGBT/FRED
Ceramic	Al ₂ O ₃	AlN	AlN	Si ₃ N ₄
Baseplate	Cu (prebent)	Cu (prebent)	AlSiC A: no prebent B: one side convex bow of 4 mils	—

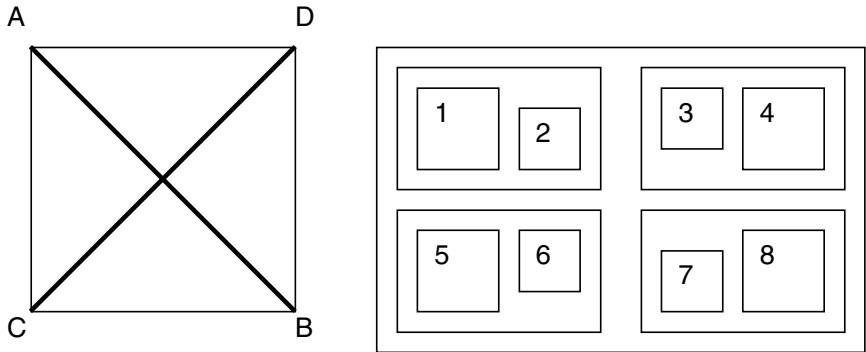


FIGURE 5.11
Diagonals AB, CD, and the physical layout.

tively by means of optical profiling. These measurements are performed at three different temperatures: -40°C , 25°C , and 125°C . This characterization provides valuable insights into how reliably a module can function at these temperature excursions.

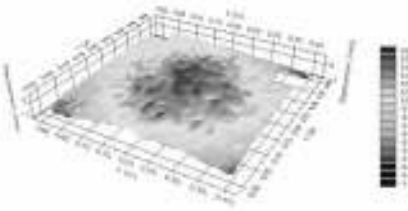
Quantitative measurements on the thermally induced warpage were performed on four samples as described in Table 5.20.

Figure 5.11 shows the physical layout of the samples. Samples 1, 4, 5, and 8 are IGBT chips, and samples 2, 3, 6, and 7 are FRED chips. Each pair of IGBT/FRED chips is soldered onto a small ceramic substrate, which is attached in turn to a large base plate. The warpage of the chips (IGBT/FRED) and the baseplate of each sample is investigated using the shadow moiré technique. The data are presented as follows:

- **IGBT (large, #1)** — [Color Figure 5.12](#) to [Color Figure 5.19](#)
 - 3D plot of the entire chip surface, -40°C , 25°C , 125°C
 - 2D plot along the two diagonals (AB: red; CD: blue), -40°C , 25°C , 125°C
- **FRED (small, #2)** — [Color Figure 5.12](#) to [Color Figure 5.19](#)

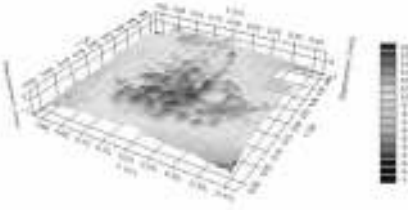
Smart Relay - Power Modules - Sample 2 - Die Surface 3D Surface Plots

T = -40°C (Large Die)



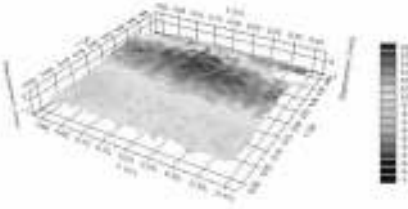
Topography: 1.5 mils.

T = 25°C (Large Die)



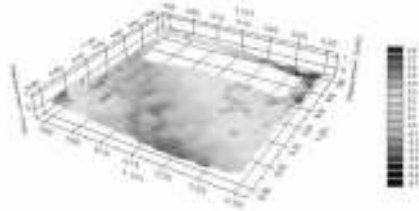
Topography: 1.5 mils.

T = 125°C (Large Die)



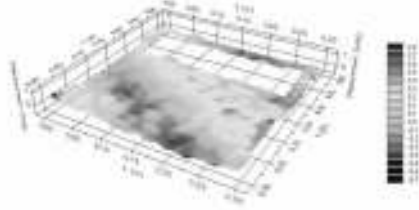
Topography: 1.5 mils.

T = -40°C (Small Die)



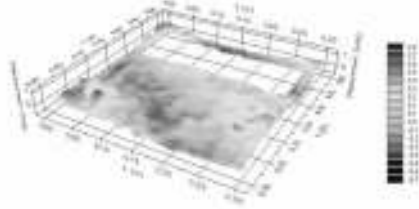
Topography: 1.2 mils.

T = 25°C (Small Die)



Topography: 1.2 mils.

T = 125°C (Small Die)



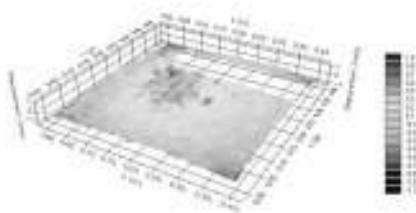
Topography: 1.2 mils.

Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.13 (See [color insert](#))
Sample 2, 3D surface plots.

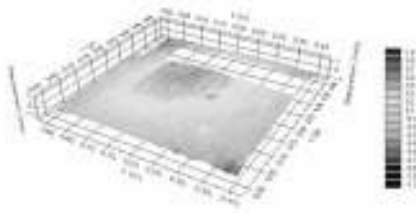
Smart Relay - Power Modules - Sample 3 - Die Surface 3D Surface Plots

T = -40°C (Large Die)



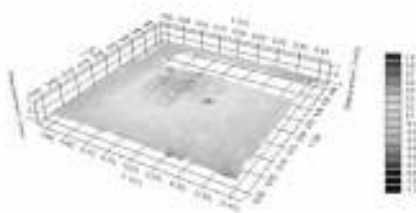
Topography: 1.57mm

T = 25°C (Large Die)



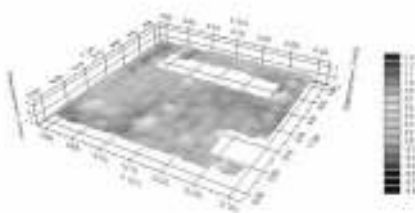
Topography: 1.57mm

T = 125°C (Large Die)



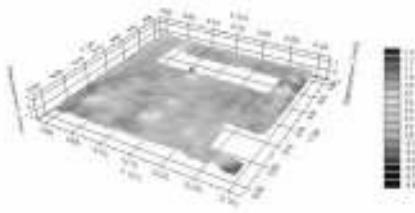
Topography: 1.57mm

T = -40°C (Small Die)



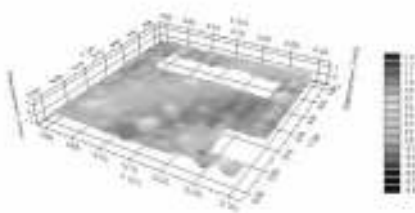
Topography: 1.57mm

T = 25°C (Small Die)



Topography: 1.57mm

T = 125°C (Small Die)



Topography: 1.57mm

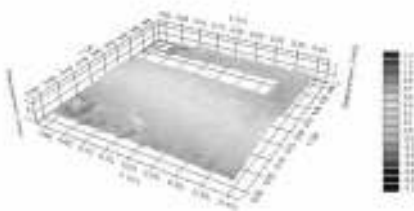
Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.14 (See [color insert](#))

Sample 3, 3D surface plots.

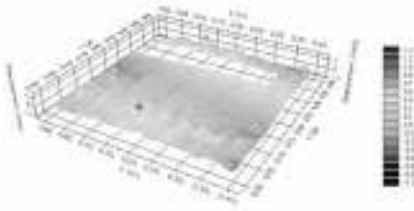
Smart Relay - Power Modules - Sample 4 - Die Surface 3D Surface Plots

T = -40°C (Large Die)



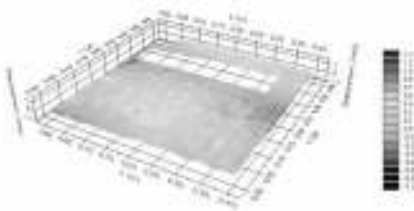
Digitally 1.23 mils

T = 25°C (Large Die)



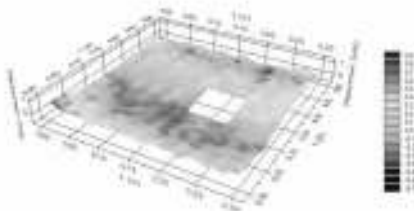
Digitally 1.23 mils

T = 125°C (Large Die)



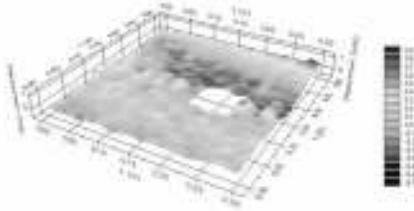
Digitally 1.18 mils

T = -40°C (Small Die)



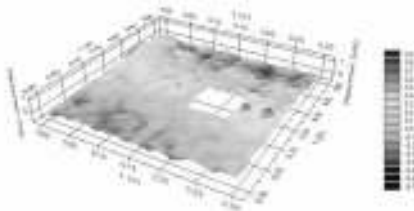
Digitally 1.18 mils

T = 25°C (Small Die)



Digitally 1.18 mils

T = 125°C (Small Die)



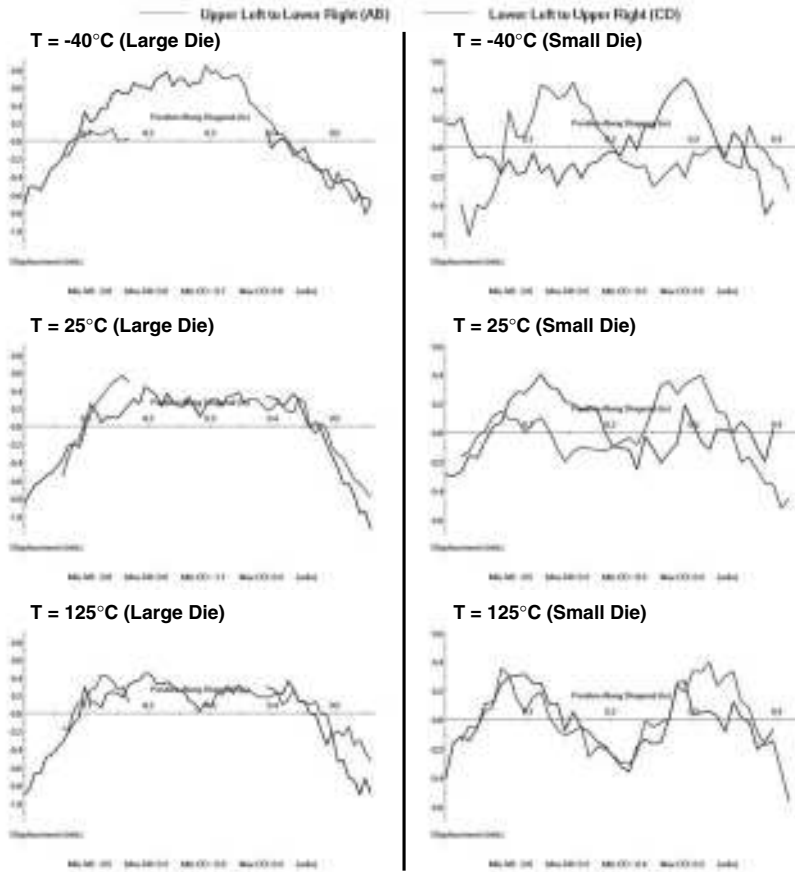
Digitally 1.23 mils

Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.15 (See [color insert](#))

Sample 4, 3D surface plots.

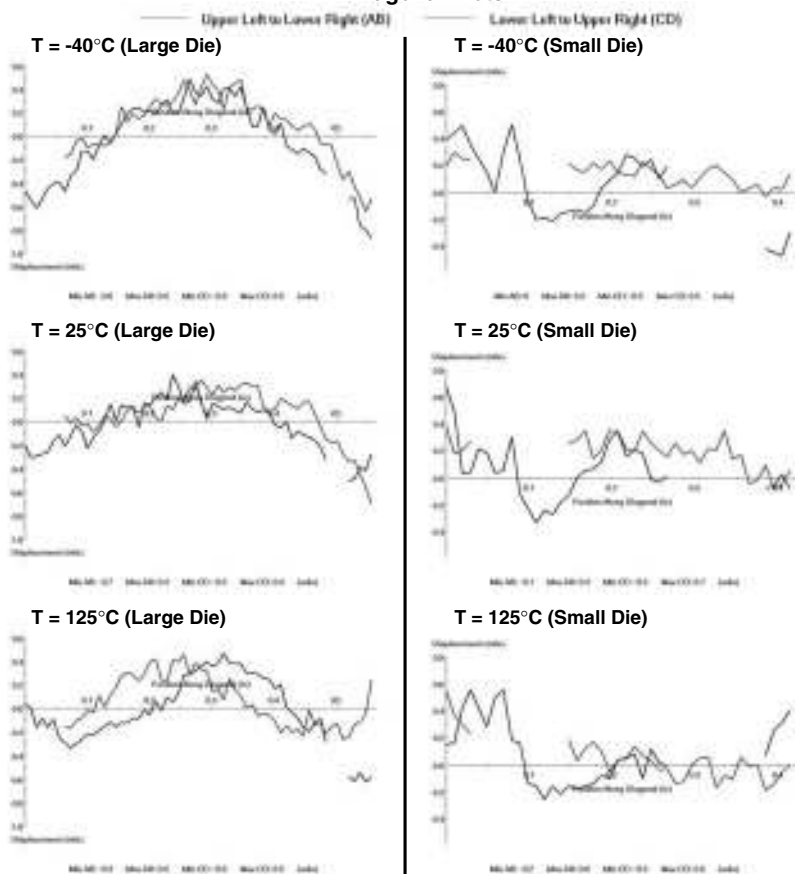
Smart Relay - Power Modules - Sample 1 - Die Surface 2D Diagonal Plots



Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.16 (See [color insert](#))
Sample 1, 2D diagonal plots.

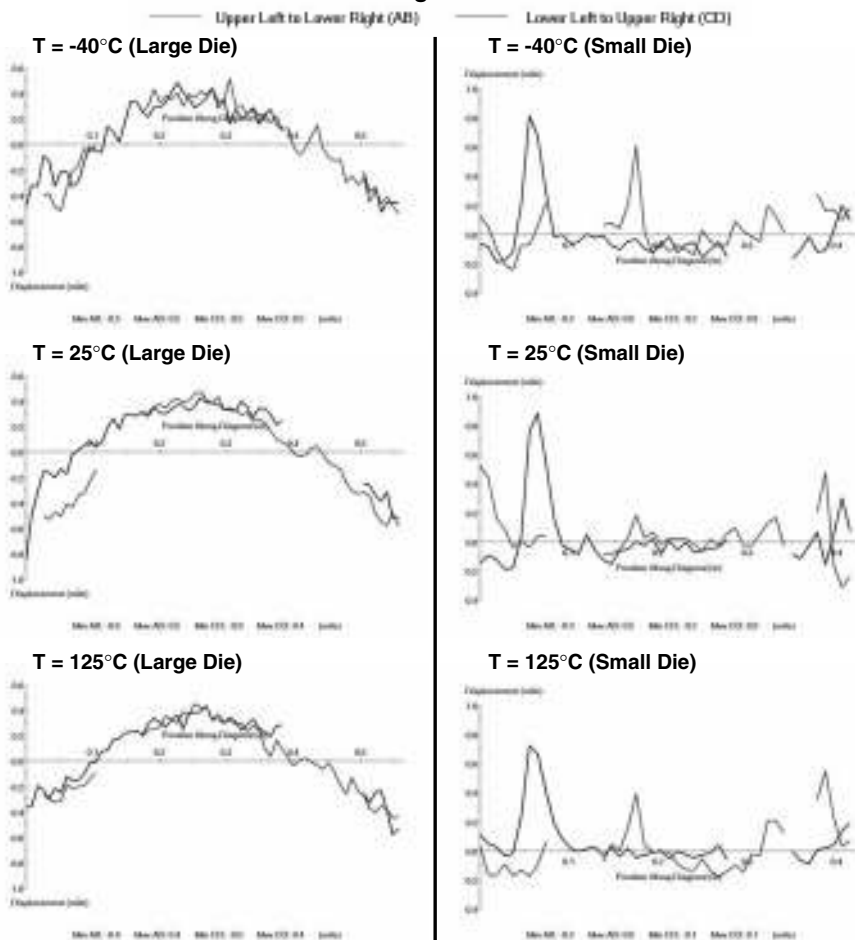
Smart Relay - Power Modules - Sample 2 - Die Surface 2D Diagonal Plots



Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.17 (See [color insert](#))
Sample 2, 2D diagonal plots.

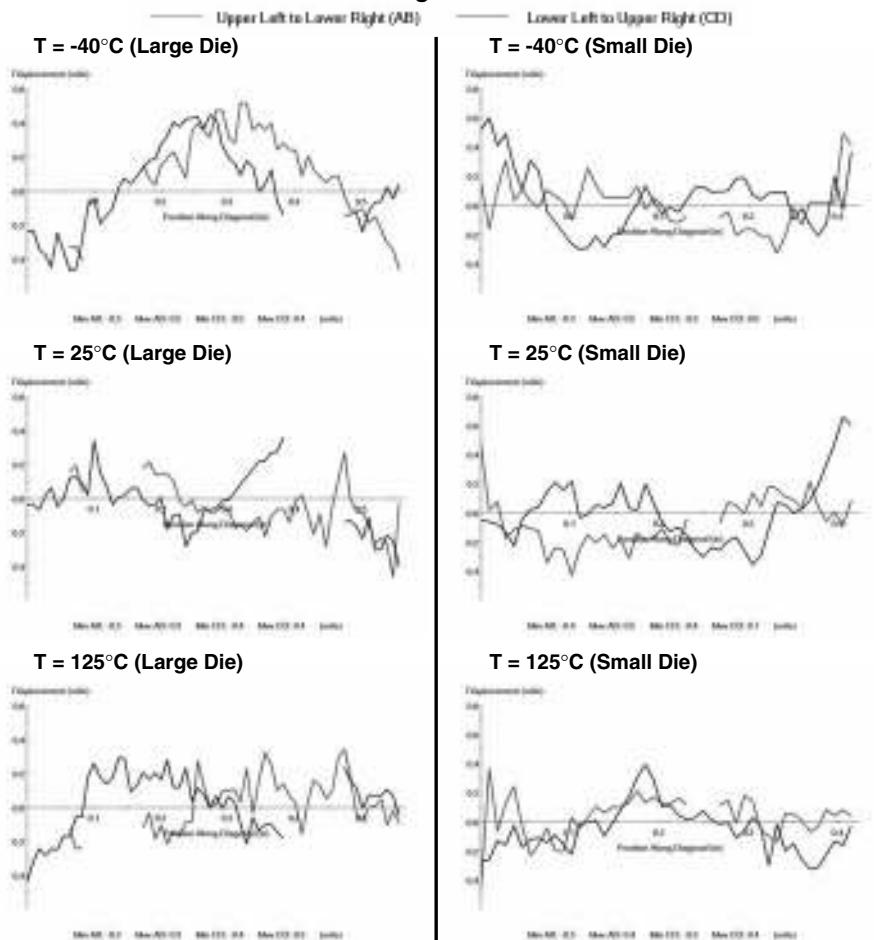
Smart Relay - Power Modules - Sample 3 - Die Surface 2D Diagonal Plots



Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.18 (See [color insert](#))
Sample 3, 2D diagonal plots.

Smart Relay - Power Modules - Sample 4 - Die Surface 2D Diagonal Plots



Results produced using the TherMoiré® Warpage Measurement System/ 2415 03-10-13

FIGURE 5.19 (See [color insert](#))
Sample 4, 2D diagonal plots.

Smart Relay - Power Modules - Sample 1 - Bottom 3D Surface Plots/ 2D Diagonal Plots

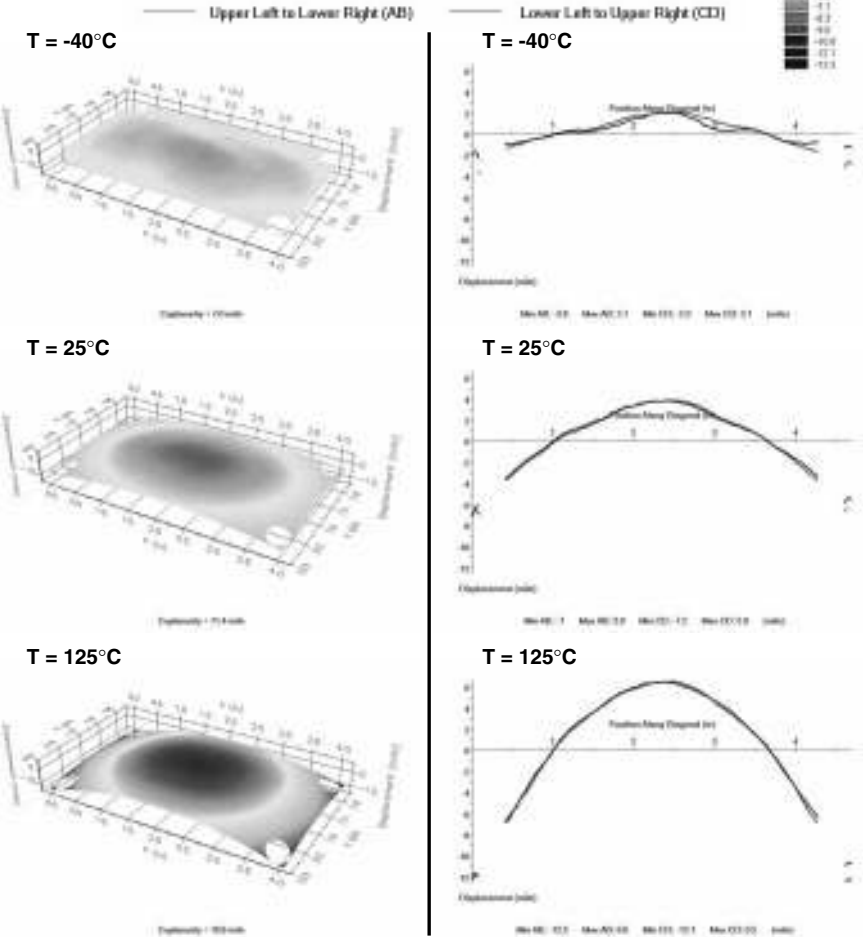
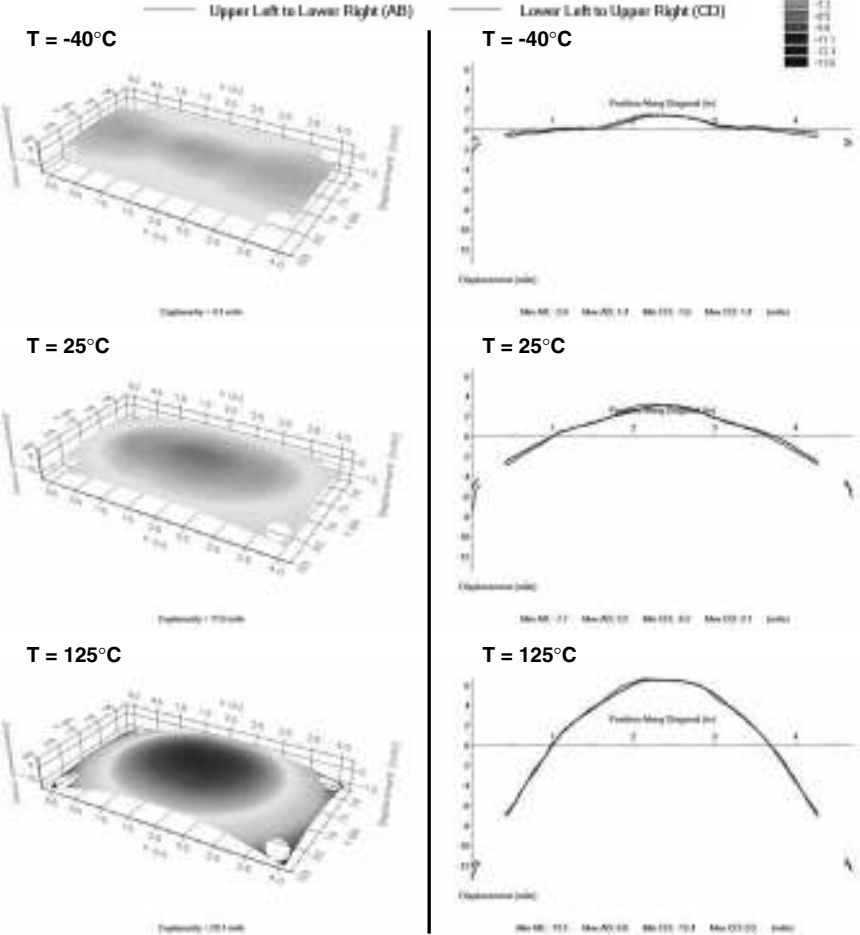


FIGURE 5.20 (See [color insert](#))
Sample 1, bottom, 3D surface plots/2D diagonal plots.

Smart Relay - Power Modules - Sample 2 - Bottom 3D Surface Plots/ 2D Diagonal Plots



Results produced using the TherMoiré® Warpage Measurement System/2415 03-10-13

FIGURE 5.21 (See [color insert](#))
Sample 2, bottom, 3D surface plots/2D diagonal plots.

Smart Relay - Power Modules - Sample 3 - Bottom

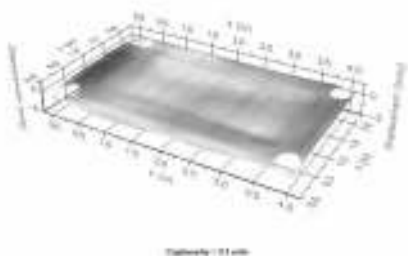
3D Surface Plots/ 2D Diagonal Plots



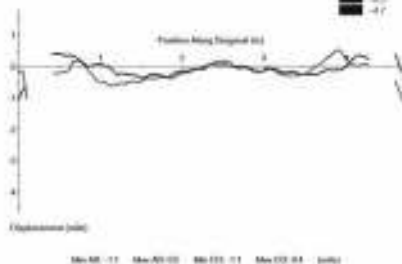
Upper Left to Lower Right (AB)

Lower Left to Upper Right (CD)

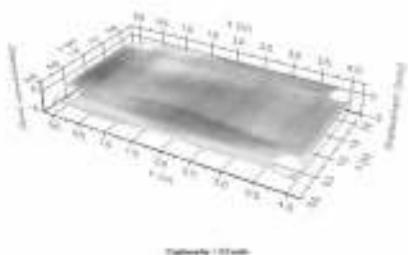
T = -40°C



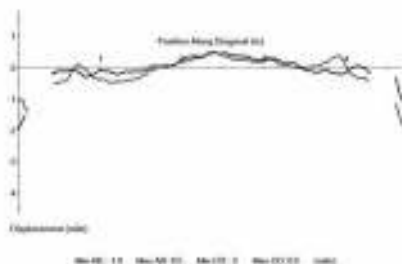
T = -40°C



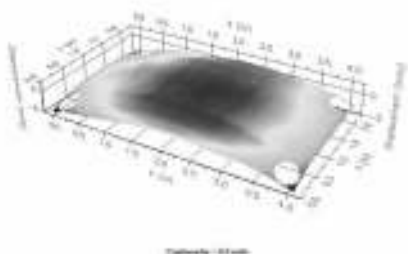
T = 25°C



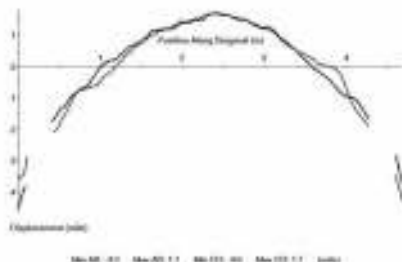
T = 25°C



T = 125°C



T = 125°C



Results produced using the TherMoiré® Warpage Measurement System/2415 03-10-13

FIGURE 5.22 (See [color insert](#))

Sample 3, bottom, 3D surface plots/2D diagonal plots.

Smart Relay - Power Modules - Sample 4 - Bottom

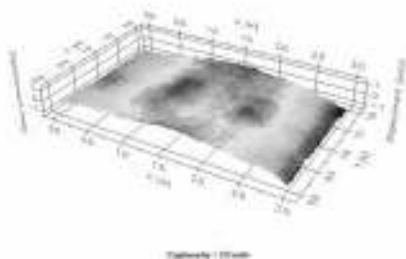
3D Surface Plots/ 2D Diagonal Plots



Upper Left to Lower Right (AB)

Lower Left to Upper Right (CD)

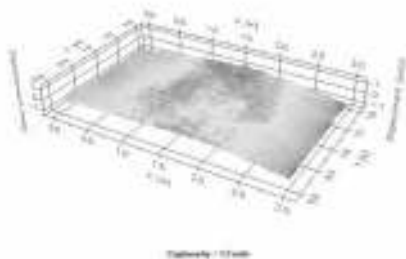
T = -40°C



T = -40°C



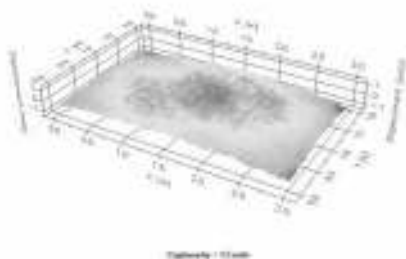
T = 25°C



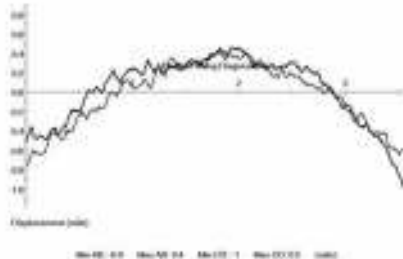
T = 25°C



T = 125°C



T = 125°C



Results produced using the TherMoiré® Warpage Measurement System/2415 03-10-13

FIGURE 5.23 (See [color insert](#))

Sample 4, bottom, 3D surface plots/2D diagonal plots.

5.4.3.1.1 IGBT/FRED Chips

- Due to mismatch in thermal expansions, all chips, IGBT (large) and FRED (small), are warped concave downward.
- The magnitude of concavity is largest at -40°C and decreases toward 125°C .
- IGBT chips show more warpage than FRED chips due to layer dimensions (Table 5.21).

TABLE 5.21
Dimensions of IGBT and FRED Chip

	IGBT	FRED
Size	0.530" $\times$ 0.530"	0.350" $\times$ 0.350"
Thickness	7–8 mils	20 mils

- The remains of the wire bonds on the chip surface can lead to erroneous readings. These will appear as isolated small bumps and must be disregarded.
- The maximum chip deformation takes place at or near the center at -40°C . Table 5.22 shows the maximum deformation of the IGBT chip for each of the four samples.

TABLE 5.22
Maximum Deformation of the IGBT Chip

Sample	Maximum Deformation (mils)
1	1.7
2	1.4
3	1.0
4	0.8

By using the following parameters for silicon chip, the displacement plots can be expressed approximately in terms of stress distribution across the entire chip surface:³

- Young’s modulus $\sim 2.35 \times 10^7 \text{ lb/in}^2$
- Poisson’s ratio ~ 0.22

On comparing this stress distribution with the maximum tensile strength as calculated from Equation 5.2, one can estimate with reasonable confidence whether a fracture may occur when the module is subjected to temperature excursions from -40 to $+125^{\circ}\text{C}$. Because the maximum tensile strength varies inversely with the flaw size, a limit on the maximum tolerable flaw allowed on the chip surface can be imposed for a particular stack structure. This simplified analysis is approximate at best, but it does provide some insight

into how reliably the module will function under different temperature excursions, without actually performing the extensive life tests. A more accurate prediction can be obtained by using finite element analysis (FEA).

The plots also provide a means to examine the thermal fatigue of the adjoining solder during the temperature excursions. Because the solder in the midsection of the chip is under the condition of almost constant stress that exceeds the solder yield strength, the Coffin–Manson model^{4,5} can be applied to estimate the solder joint life (crack initiation point):

$$N_f \equiv \frac{1}{2} \left(\frac{\Delta \epsilon}{\epsilon_f} \right)^{-2} \tag{5.7}$$

where

- N_f = Number of cycles to failure
- $\Delta \epsilon_f$ = Range of plastic strain created due to the displacement differentials between the two adjoining components
- ϵ_f = Fatigue ductibility coefficient (For eutectic and near-eutectic solders, $\epsilon_f \sim 0.65$.)

Once the crack has initiated, growth and failure are rapid. On the other hand, if cracks already exist in the solder, the solder joint life is controlled by the growth of these cracks. In this case, the fatigue life would be much shorter. *Inspection for solder cracks is therefore crucial.*

5.4.3.1.2 Baseplate

- The measurement is performed with the bottom surface of the baseplate facing up.
- Due to the thermal mismatch, the convexity is largest at 125°C and smallest at –40°C. Table 5.23 shows the displacement of the baseplate for different samples.

TABLE 5.23
Displacement of the Baseplate

Sample	Displacement (mils)	
	25°C	125°C
1	11	20
2	11	20
3B	3.3	6.3
4	1.3	1.5

When the baseplate is bolted to the heat sink at four corners, there is a tendency to bend the plate upward — in other words, concave toward the heat sink. The convexity of the baseplate must be large enough to overcome this concavity tendency; otherwise, the baseplate cannot make intimate contact with the heat sink for effective dissipation. From the thermal impedance measurements, it is found that samples 1, 2, and 3B behaved well at the heat sink interface, whereas sample 4 failed.

5.4.3.2 Thermal Impedance Characterization²

This is basically a heating step-response test. Here, the thermal impedance of the module is plotted against the heating step duration. It provides the following useful information about the thermal behavior of the module from transient to steady state.

- Transient (10 to 100 ms) — Determine peak current, I_p , capability.
- Steady state (> 500 ms) — Determine continuous current, I_C , capability.
- Evaluate solder attachment of different layers.
- Identify the contributing factors to thermal impedance.
- Establish the best heating pulse duration for chip attachment screening.

Figure 5.24 shows the heating curves of the five samples mounted on a water-cooled heat sink with thermal grease at the interface.

An examination of these curves will provide some insight on the rate of heat flux through the IGBT stack. For the first 10 to 12 msec, the heat flows through the IGBT chip and enters the chip-attachment region. During this time, temperature rises are almost entirely controlled by the thermal spreading in the chip region. Samples 1, 2, 3A, and 4 behave in the same manner and all have good IGBT chip attachment. Sample 3B, however, appears to have poor attachment.

The heat then travels almost vertically through the ceramic substrate in the next 40 to 60 msec. Sample 3A continues to track well with sample 2, as it should. Sample 3B starts to deviate from its normal course. Samples 1 and 4 also show high thermal impedance due to the poorer thermal conductivities of Al_2O_3 and Si_3N_4 . At about 60 msec, the heat enters the baseplate and starts spreading three-dimensionally. Here, the Cu's high thermal mass and conductivity become evident. These thermal characteristics are clearly illustrated by the divergence of samples 2 and 3A and the crossover of samples 1 and 3A. The thermal resistance of sample 3A is further degraded by the fact that its AlSiC baseplate is not prebent. This results in a negative-convex structure that prevents intimate contact with the heat sink and yields a thermal resistance to ambient much higher than

expected. Sample 3B, on the other hand, has a one-sided convex bow, and this results in a distinct improvement in the heat dissipation through the heat sink. Sample 4 has no baseplate and should, theoretically, produce the best thermal resistance. However, because no special attempt has been made to control the warpage, the final structure shows a slight positive convexity but not enough to compensate for the concavity created during screw mounting. For this baseplate design to function properly, the ratio of the top-to-bottom Cu metallization must be optimized to give a positive convexity of about 3 mils.

Detailed analysis of the interface thermal resistance must involve surface profile, surface roughness, and contact pressure.⁶ Table 5.24 shows how the results of these five samples compare with calculations.

TABLE 5.24
Comparison with Calculation of Sample Test Results

Sample	Comparison with Calculation
1, 2	Good for the entire stack (within 10%)
3A	Good for chip and ceramic Poor for case and heat sink
3B	Poor for chip Good for ceramic and case to heat sink
4	Good for chip and ceramic Poor for ceramic to heat sink

The preceding heating curves can be modeled by a third-order R–C network,² shown in [Figure 5.25](#).

TABLE 5.25
R and τ for Different Samples

	Sample				
	1	2	3A	3B	4
R_1 (°C/W)	0.021	0.027	0.027	0.039	0.024
τ_1 (sec)	0.00201	0.00342	0.00395	0.00672	0.00326
R_2 (°C/W)	0.068	0.064	0.094	0.072	0.177
τ_2 (sec)	0.06802	0.1939	0.2657	0.09935	0.2401
R_3 (°C/W)	0.050	0.027	0.067	0.052	0.053
τ_3 (sec)	1.2047	3.3372	3.1768	1.1813	2.1614

- R_1 ~ Thermal resistance of IGBT chip attachment region
- R_2 ~ Thermal resistance from chip attachment region to the baseplate region
- R_3 ~ Thermal resistance from the baseplate region to ambient environment

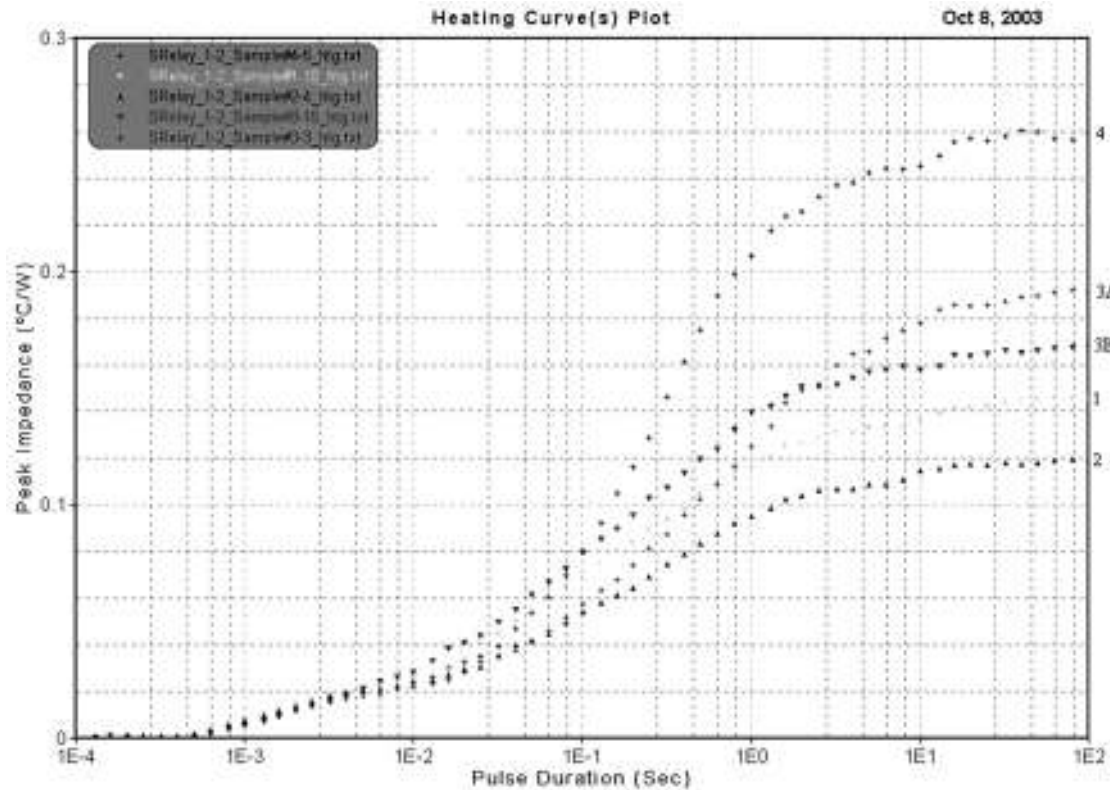


FIGURE 5.24
Composite heating curve (plot).

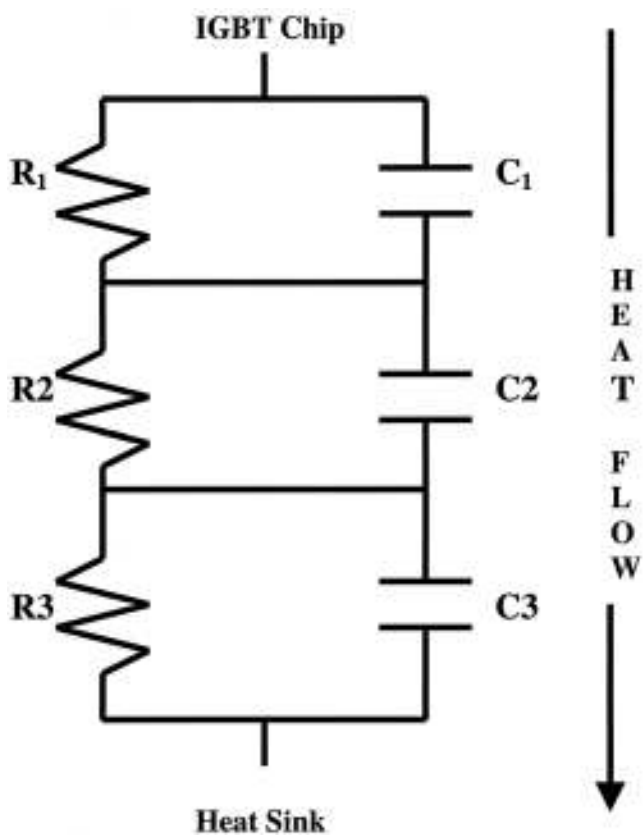


FIGURE 5.25
Thermal model for the IGBT stack.

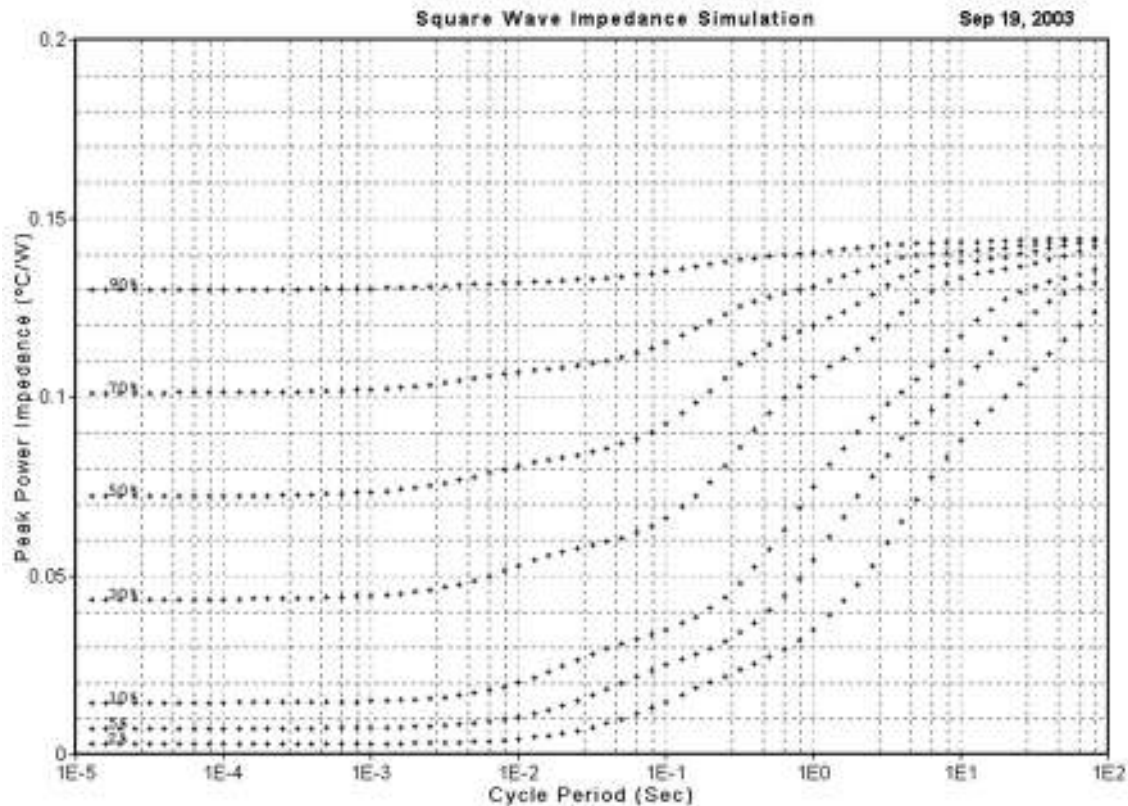


FIGURE 5.26

Sample 1, square wave impedance simulation.

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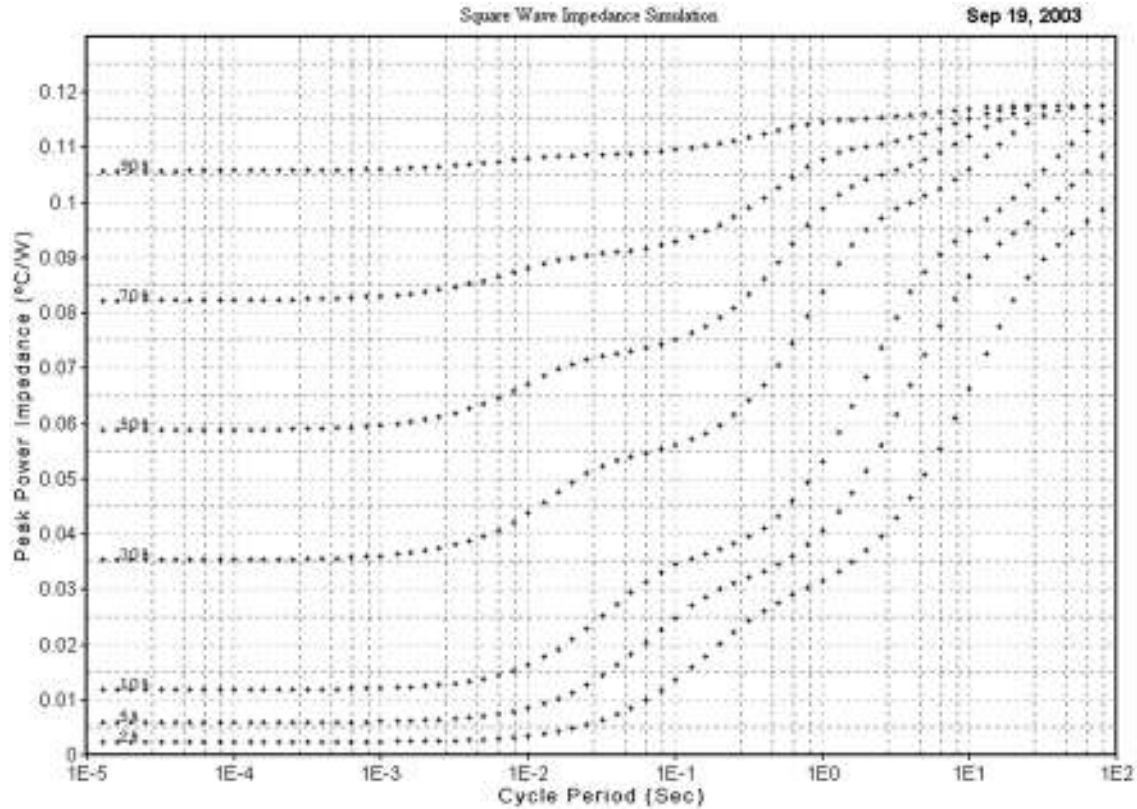


FIGURE 5.27

Sample 2, square wave impedance simulation.

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C1, C2, and C3 represent the corresponding heat capacitances of the regions. These regions are not well defined and may or may not be the same as the actual physical boundary of the stack layer. The rate of heat flow can be expressed in terms of the time constant, τ , or RC.

Table 5.25 shows the R and τ values for fitting the four heating curves of Figure 5.24.

These parameters also provide the ability to simulate the device's thermal behavior under various frequency and duty cycles. The results for the samples 1, 2, and 3B are shown in Figure 5.26, Figure 5.27, and Figure 5.28, respectively.

It is hoped that the measured data presented here will serve three purposes:

- Criteria for manufacturing inspection
 - Chip attachment
 - Chip concavity
 - Baseplate convexity
- Aid for examining the internal thermal resistance and the transient thermal behavior of the stack
- Guide for engineering design

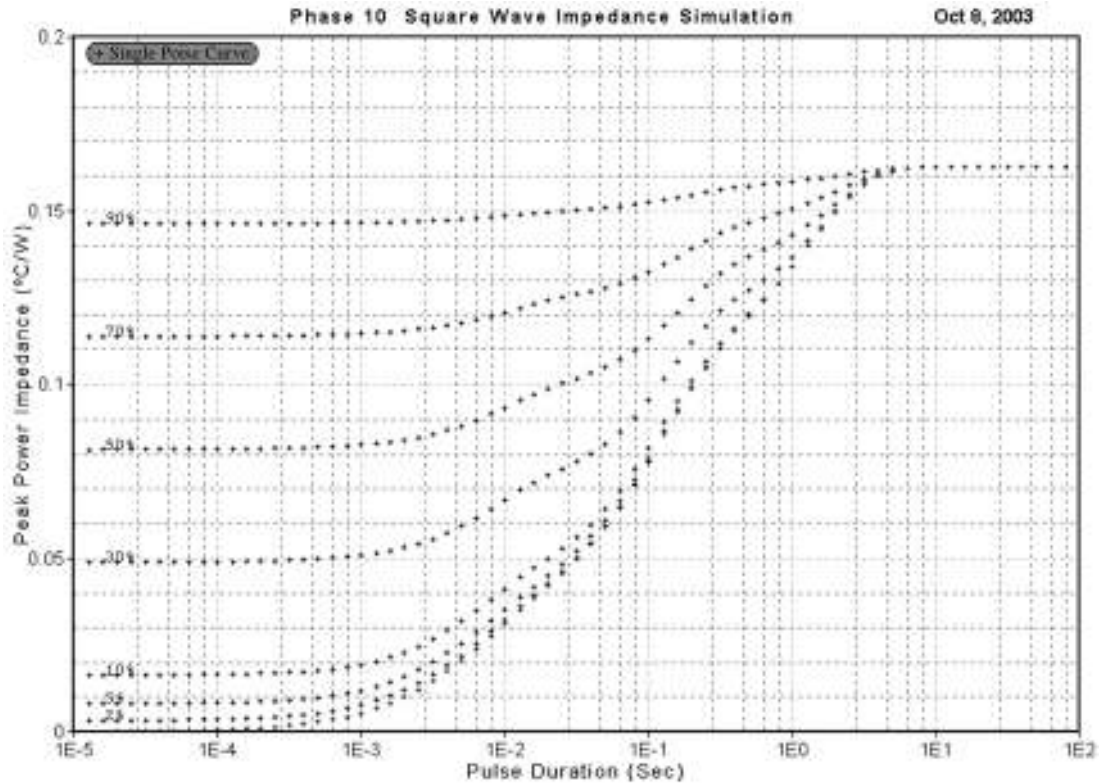


FIGURE 5.28
Sample 3B, square wave impedance simulation.

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Appendix B

Barcode and 2D Data Matrix Symbol

A product ID in the form of a bar code can be set up to store information regarding traceability and performance characteristics. This can be attached to the plastic case as part of a label. Besides the bar code (linear or stacked), a 2D data matrix symbol can also be used. This symbol has size ranges from 10×10 (rows $\times$ columns) with an alphanumeric data capacity of 3 to 144×144 , where the capacity increases to 2335. For a standard IGBT module without any special testing requirements, a symbol of 44×44 (roughly 0.50×0.50 " in physical size) with 214 alphanumeric data capacity should be sufficient to include:

- Lot #
- Serial #
- Date manufactured
- Testing data:
 - Electrical — static, dynamic, short-circuit
 - Thermal
 - Mechanical

Numerous bar code/2D data matrixes generating and printing software created with programs such as MS Word, etc. are available. Suppliers for such programs and scanners include the following:

- Taltech Betasoft
- Tharo Systems
- Teklynx (code soft for 2D data matrix)
- Microscan (scanner for both bar code and 2D data matrix)